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Silicon Carbide Megawatt Power Devices for Combat Vehicles

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13. ABSTRACT (Maximum 200 words)

This report documents the impact of the Megawatt Program on SiC power development. The executive summary section contains an extensive discussion of the program objectives, technical approach, technical challenges, development tasks, program accomplishments, transition and scientific results. This program has advanced the SiC power device technology on many fronts spanning from devices to applications. Specifically, high performance PiN diodes, GTOs, DIMOS and MGTs were designed, simulated and characterized; manufacturable processes for PiN diodes and GTOs were developed; their static and dynamic performance was evaluated; Si and SiC hybrid half-bridge inverter modules were fabricated; and novel application concepts for SiC power devices were formulated and analyzed. The knowledge accumulated under this program was shared with the sponsor and the DoD community at first and then published to accelerate the technology transition.

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IV. Acknowledgements

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Foremost, we recognize the leadership role of government agencies, which created a vital community around this program. We greatly benefited from suggestions and constructive feedback from our sponsors, who coordinated multiple programs to reach a common goal. Dr. Elliott Brown, DARPA, started the program and provided the initial justification, set the goals, and guided its execution for the first year. Dr. Daniel Radack, DARPA, continued the program and managed it through the technology transition phase. Dr. George Campisi, ONR, was the technical leader most frequently in contact with the development team to offer suggestions and advice. Dr. Terry Burke, US Army TACOM, established the link between the program results and the Army needs. Dr. D. Larkin, NASA, demonstrated the program feasibility with his fundamental research in silicon carbide (SiC) epitaxy and assisted us with samples and advice throughout the program.

The contributions of many external organizations were necessary to complement the tasks and capabilities of the prime contractor, General Electric Corporate Research and Development (GECRD). Fortunately, leading engineering departments of major US universities provided their support in their area of expertise of SiC technology. Specifically, Prof. T.P. Chow, Rensselaer Polytechnic Institute (RPI), and his team developed novel device physics. Professors S. Saddow and M. Mazzola, Mississippi State University (MSU), contributed thick layer epitaxy and silane overpressure annealing. Prof. M. Rao, George Mason University (GMU), conducted high-energy implantation studies. Prof. M. Capano, Purdue University, investigated MOS gate formation.

An equally important contribution was made by many industrial companies, which worked on this program to build the infrastructure for bringing SiC High Power devices to the market and into applications. Cree, Inc. provided advanced epitaxial wafers before they were commercially available to satisfy our novel device design. Omnirel, Inc., Lockeheed Martin Control Systems and Sinclair, Inc., assisted with discrete packaging of individual devices at high voltage and high temperature. Powerex, Inc. developed a SiC/Si hybrid power module, which is a one-to-one replacement of existing Si ones. Lockheed Martin Missiles and Control Systems funded the development of a stretched program goal, that is the design and fabrication of a 10 KV SiC diode, which proved very useful to extend the technical knowledge beyond the cliff of the program goals and related design specifications. Jet Process Corporation (JPC) studied the possibility of using the jet vapor deposition process to improve MOS gate oxide reliability on SiC devices.

At GECRD the multidisciplinary nature of this program brought together many technical contributors from various departments. We recognize first of all the fabrication team, i.e. J. Kretchmer, P. Gipp, and M. Lazzeri; the measurement team, i.e. J. Garrett, M. Nielsen,

D. Cusano and D. Hanchar; the layout designer, J. Richotte; the functional testing team, i.e. A. Elasser, W. Clock, and J. Park; and the application team, A. Elasser and M. Kheraluwala.

A special thanks to GECRD managers R. Kolc and D. Walker for their enthusiastic support of this program, which in their view is a cornerstone for advanced GE electrical system products. Dr. Dale Brown made a major contribution to shaping the proposed statement of work and was always ready to advice and contribute his vast experience to this program.

The program complexity, tight schedule and ambitious goals challenged the ability and dedication of the Principal Investigators, i.e. Mario Ghezzo, Nikhil Taskar and Stephen Arthur. We especially recognize their efforts to coordinate many subcontractors and to lead them toward common objectives within the program constraints.

Finally, we thank GECRD's publication team for helping with the preparation of the contract proposal, viewgraphs, interim reports and the final report. These efforts improved the communication effectiveness and the understanding of the technical results by a wider readership. We particularly thank Dr. Russ Clark, Carl Filbrich and Tom Mangano for their editorial efforts.

In such a large program we humbly recognize the potential for oversights of important contributions. We apologize for these shortcomings and we ask forgiveness from those that we inadvertently did not acknowledge here.

1. Executive Summary

In recent years power electronics has made significant advances creating new opportunities for applications once reserved exclusively for mechanical systems. In the case of combat vehicles, old models used nearly exclusively mechanical gears and hydraulics for propulsion and control functions. Electronics was used only for communications, navigation, engine starting, fuel pumps and lighting. These uses required only modest power ratings, which were within the capabilities of first generation power devices.

The next generation of combat vehicles is facing operational challenges, which cannot be met with a conventional design. Novel strategies for deployment of tanks and scout vehicles require higher mobility, increased lethality, stealth operation, airlift capability and high reliability with low lifecycle cost. The proposed solution is to develop a hybrid propulsion system with electromechanical controls. Moreover, novel weapons will be employed, such as high kinetic energy electromagnetic guns and direct-energy laser guns. The result will be an unprecedented need of electric energy for both continuous and pulse power mode.

The control and distribution of such a large amount of power will require rugged power semiconductor devices with high power rating in the megawatt range, low static and switching losses, high frequency operation, and high temperature. For pulse power armaments, such as laser and electromagnetic guns, an additional requirement is high peak current and voltage in the gigawatt range, and high di/dt and dv/dt.

Traditionally, electronic designers have used Silicon (Si) based devices for motor drives and high power vacuum tubes for microwave and laser weapons. Unfortunately, the efficiency of Si power devices drops significantly at high voltage and high frequency. Moreover, their upper temperature limit is 125 °C for military use. Vacuum tubes are large, less reliable than solid-state devices, and consume large stand-by power. Therefore, none of these devices is a good choice for the next generation of advanced combat vehicles.

A wide bandgap semiconductor, Silicon Carbide (SiC), promises to overcome these Si limitations by virtue of its physical properties. Although SiC high power device capabilities have been theoretically predicted, only now they are being verified with the development of SiC power device technology. This program is a major effort in this direction with emphasis on power devices suitable for combat vehicles.

The program developed and demonstrated in SiC (1) PiN diodes of 5000 V/5A; (2) Schottky diodes of 800 V/5A; (3) GTOs of 800 V/1A. A hybrid power module composed of a SiC diode and a Si IGBT was developed using a package fully compatible with an all-Si commercial power module. Specialized switching measurement circuits were developed and used to provide a complete characterization of the new devices at meaningful current and voltage levels for proposed applications. Since interim results were reported and exchanged within the SiC power device community, the progress rate

was faster and led to the formation of an infrastructure including material growers, device developers, packaging experts, circuit designers and application engineers.

However, despite these achievements, the program also showed many weaknesses of the present technology status. These must be overcome before SiC power electronics will become commercially available. Among the key challenges, even for simple diodes, there is a need to increase the yield of large area devices to produce affordable SiC components with high current and blocking voltage. For this reason, higher quality SiC material and processing are needed. Other challenges are in the area of packaging. High temperature (350 °C) packages of > 5000 V and >200 A are needed to take advantage of the SiC high temperature capability and allow a higher heat dissipation rate to achieve a higher system efficiency. Moreover, circuit simulator models of the new SiC devices must be developed to offer the circuit designers a choice between Si and SiC devices for their applications.

1.1. Program Objectives

The program objectives were drafted in response to DoD power electronic needs and SiC technology status as they were at the beginning of the program in 1997. Until that time the main SiC research efforts were aimed at improving the crystal quality and reducing the defect density, especially micropipes. Various types of bipolar and MOS devices had already been demonstrated, but their size was too small to be of any value for a power circuit demonstration. Moreover, there were many doubts on the ability of achieving a sufficiently high yield to justify economically the new technology.

There were also debates on the application drivers of the emerging SiC technology. In addition to the well-established use for blue LEDs, high emphasis was placed on high temperature operation of small diodes and signal amplifiers, especially MOS devices, to exploit the SiC wide bandgap for high temperature sensors. On the other hand, research

Table 1-1. Program objectives

- Develop a comprehensive suite of SiC high-power electronic components for combat vehicle power systems
  - Hybrid propulsion for vehicle traction
  - Pulsed power for weapon systems
- Develop active SiC solid-state switches with blocking voltage of 5000 V and 200 A current rating at 150 kHz
- Develop a SiC high-power device technology for high temperature operation up to 350 °C for reduced external cooling
- Develop devices and fabrication processes that are scalable to higher current/voltage ratings as SiC material quality improves
- Demonstrate a basic SiC high-power building block by designing and fabricating a half-bridge module with the new SiC devices

on power devices had just started based on modeling predictions of SiC superiority over Si for high voltage and high power operation due to its 6-10x higher critical electric field. Theoretically, this results in lower specific on-resistance for the same blocking voltage, and hence as much as 40x reduction of power dissipation. DARPA quickly recognized this advantage and sponsored the Megawatt initiative, where a main goal was to demonstrate the potential use of SiC power electronics for the next generation combat vehicles. The objective was to develop robust SiC power devices with high current and voltage ratings and to build a successful power circuit as a technology demonstrator. These requirements determined the specific program objectives, which are listed in Table 1-1.

Aboard a combat vehicle high power electronics is used both for propulsion and weapon systems and requires continuous and pulse power operation, respectively. Considering the weight and acceleration of a tank, it follows that the propulsion motor drive ratings must be in the megawatt range with frequency of 10-100 KHz. Conversely, kinetic and laser weapon systems require high energy pulses in the megajoule range, which translate into gigawatt device ratings and very high di/dt and dV/dt, but with low duty cycle, typically <1%. Hence, the first program objective was to develop a comprehensive suite of rectifiers and switches, which could be evaluated for both modes of operation. However, to be within the time and budget constraints, the end objective was to limit the circuit demonstration to a motor drive basic building block, that is a half-bridge inverter.

Another objective was to develop devices, which would better exploit the properties of SiC yielding a performance increase at the system level. For this reason, the required megawatt power rating was partitioned into high voltage (5000 V) and relatively low current (200 A) specifications. As explained earlier, SiC devices have an edge over Si at high voltage, but cannot be made yet with large area, as required for high current rating, because of high material cost and defect density. Nevertheless, it was recognized that design, layout and fabrication processes are scalable to larger area devices as soon as the material quality will improve. Therefore, one objective was to generate a vast learning experience for device technology readiness for future use.

Besides the high critical electric field, the other two SiC properties, which have a major bearing on power devices, are its wide bandgap (3.0 eV) and high thermal conductivity (5 W/K cm). A wide bandgap allows to operate safely at high temperature with low leakage, while a high thermal conductivity increases the heat dissipation rate. This is further enhanced by the larger temperature difference between device junction and heat sink, which is associated with high temperature operation. Therefore, a program objective was the development of the device and packaging technology necessary to operate the new devices on a wide temperature range up to 350 °C. This upper limit is not intrinsic to SiC, but mainly determined by the eutectic temperature of the die bonding alloy used for packaging. It is also an accepted conventional first step in the quest for higher temperature, which compromises between the benefits of high temperature for system thermal management and the still unsolved temperature dependent device and packaging reliability issues.

1.2. Technical Approach

The technical approach was chosen in accordance with the program objectives. Additional decision elements were the status of SiC technology at the beginning of the program, the capabilities and experience of our team, the sponsor's requests and the desire to minimize risk without compromising the technical achievements. Nevertheless, as the program evolved, there were many external developments, which affected the initial plan and led to changes of the technical approach. For instance, MOS-based devices proved to be much harder to develop than originally thought shifting more resources to bipolar devices, because they appeared closer to transition.

As indicated earlier, the overall program objective was to develop a comprehensive suite of SiC devices for demonstrating a half-bridge power circuit with current and voltage ratings suitable for electric propulsion of a combat vehicle. Hence, the planning process started by drawing a schematic diagram of the proposed half-bridge module to determine the devices needed and their specifications.

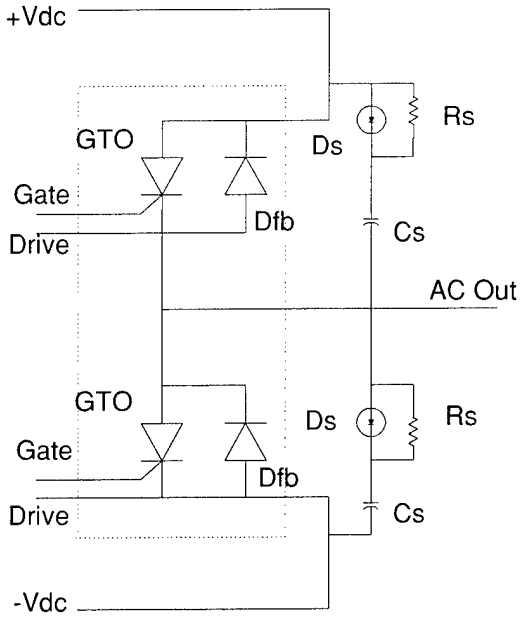


Figure 1-1. Half-bridge circuit

Figure 1-1 shows the schematic of the half-bridge circuit. It consists of two SiC GTO devices connected in series along with two flyback diodes, Dfb, to form a half-bridge "leg". Using this building block approach, many types of power converters can be configured. For example, three such modules can be used to implement a three-phase inverter for motor drives. For higher power drives, current capability above the single-device 200 A rating may be achieved either by paralleling power modules or by paralleling individual devices with a single power module. The analysis of the optimal method is part of the program.

Figure 1-1 also shows additional "snubbing" devices for decreasing dv/dt and di/dt stresses on the main switches. These are the diodes, Ds, resistors, Rs, and capacitors, Cs. Moreover, to drive the GTOs, gate drivers are needed, which are typically MOS power devices. Their choice allows a voltage drive with a high-input impedance for optimal coupling to the motor controller.

The need of a snubber complicates the fabrication of the half-bridge module, because of the presence of passive components Rs and Cs, which must also withstand the high temperature operation allowed by SiC devices. Since development of high temperature passive components was outside the scope of this program, it was decided to use existing

passive components and to reduce the upper temperature limit of circuit operation to 250 °C.

With regard to measurements, the most desirable approach is to characterize the half-bridge module in a dynamic mode by connecting two half-bridge circuits in a full-bridge configuration to an inductive load, which represents the motor windings. However, contemplating the possibility that the specified device ratings would not be achieved or that fewer modules would be available, a fallback position was planned. This consisted of measuring the half-bridge transient characteristics on a specially built test circuit. The latter approach was eventually adopted after low device yield coupled to material and fabrication delays prevented to carry out the most complete characterization.

Table 1-2. Choice of SiC power devices

Planned SiC Power Devices	Use	Issues
SiC Schottky Diode (100 V, 100 A)	Snubber diode	• Schottky barrier metal • Junction termination • Metallization • Defect density
SiC PN Diode (5000 V, 200 A)	Flyback diode	• SiC lifetime • N- epi layer thickness > 40 μm • Junction Termination Extension (JTE) • Activation of P-type implants • Low contact resistance to anode
SiC GTO (5000 V, 200 A)	Main switch	• SiC lifetime • 4 to 5 epi layers of alternating polarity • Buffer layer over N+ substrate • Deep trench etching • Accurate epi doping/thickness control
SiC DIMOS FET (100 V, 100 A)	Gate driver	• Gate oxide reliability • Low interface states • Threshold voltage control • Effective channel mobility • Channel length uniformity and control • Activation of implanted P-base
SiC MOS Gated Transistor (MGT) (5000 V, 200 A)	Main switch (option)	• Novel device • Multiple N and P implants • High voltage planar MOS • All DIMOS problems

Table 1-2 lists the devices required to implement the half-bridge. Next to each device, there is a list of the most prominent issues associated with that device. In addition, there are common issues, which are shared by all the devices, such as low yield due to high SiC defect density and lack of adequate doping uniformity. As a consequence, the current ratings achieved during the program were well below the target specifications of 100-200 A, because of sharply declining yield with increased chip area.

To fabricate these devices we had to select between the mesa and the planar approach. With the mesa approach the various doping and polarity regions are formed by epitaxial layers, which are then partially exposed by deep etching to make external electrical contact. With the planar approach ion implantation is used to form the various device regions by selectively changing the doping concentration and polarity of a lightly doped substrate without affecting the surface planarity. Both approaches have pros and cons, which are largely dependent on the maturity level of a technology and the basic semiconductor properties. For compound semiconductors, the mesa approach has been used first, mainly because of lack of experience with ion implantation and dopant activation. On the other hand, mesa etching often leaves residues in the trenches and may cause reliability problems due to inadequate metal and oxide step coverage.

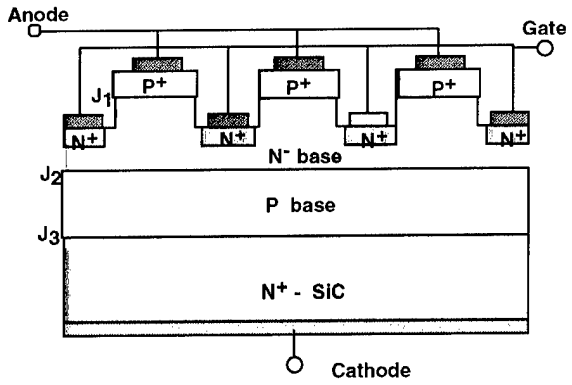


Figure 1-2. SiC GTO

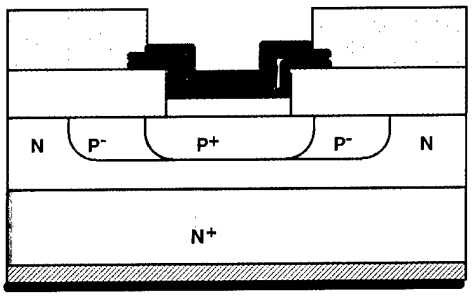


Figure 1-3. SiC planar PiN diode

We selected the mesa approach for the GTO and the planar approach for the other devices. A GTO structure consists of a stack of up to five differently doped regions with only one internal region connected to an external terminal, as shown in Figure 1-2. Hence, multiple epi layers are necessary to form this structure with a relatively simple surface topology. These features favor the choice of a mesa approach. Instead, high voltage PiN and Schottky diodes have a simple vertical structure, but with many lateral doping variations to form the anode and the junction termination extension (JTE). The planar approach is therefore more convenient and potentially cheaper, because of the selective masking capability of ion implantation and the lack of surface steps. A planar SiC PiN diode is shown in Figure 1-3.

In the case of MOS-based devices, i.e. DIMOS and MGT, the channel characteristics hold the key to their

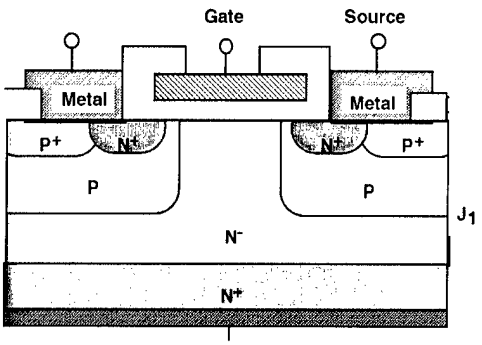


Figure 1-4. Planar SiC DIMOS

electrical performance. Figure 1-4 shows the cross-section of a planar SiC DIMOS. Our past experience using the mesa approach for these type of devices resulted in high interface states density, very high threshold voltage and unacceptably low channel mobility of the MOS channel formed on the trench sidewalls. It was also very difficult to control the etching depth with regard to the epi junctions, because these processes act in opposite directions, while the errors are additive. Therefore we selected the planar approach to facilitate the channel formation and use our large knowledge base already accumulated on SiC MOS low voltage signal transistors. However, in planar DIMOS devices the channel is formed on an implanted p-base. This factor proved to be very detrimental to device performance, because of residual damage in ion implanted regions, especially p-type, thereby preventing the formation of a high quality MOS interface and channel. Nevertheless, there is hope that in the future either a new annealing process, called "silane overpressure", or a device structure modification may overcome these problems.

The selection of a GTO as the half-bridge main switch has been heavily debated, because circuit designers preferred an IGBT. Their argument was that today in silicon technology GTOs are being replaced by IGBTs, because of higher switching frequency, voltage gate drive, reduction of snubbers, and easier implementation of hard switching techniques for motor drives. Unfortunately, the IGBT advantages will be realized only when the SiC MOS technology will reach its theoretical potential, which appears still an elusive target.

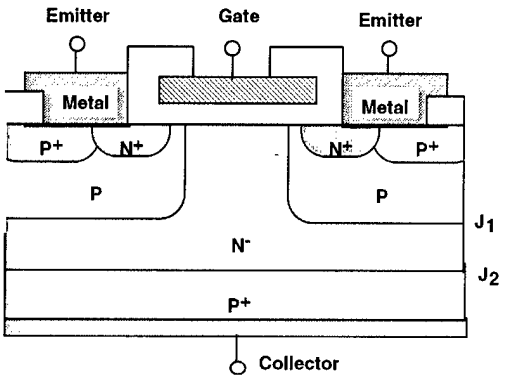


Figure 1-5. N-channel SiC IGBT

Of the dual possible choices of IGBT polarity, the N-channel IGBT is the most sensible choice to obtain a sufficient channel gain considering that in SiC the effective MOS channel mobility is already very low even for electrons. This leads to the device structure shown in Figure 1-5. Unfortunately this requires a P+ substrate, which raises significantly the lower theoretical limit of specific IGBT on-resistance due to the ~10x lower hole mobility in SiC compared to electrons. Additionally, in this IGBT the main transistor is of pnp type, which in SiC exhibits a lower open-base breakdown voltage, BV_{ceo}, than an equivalent npn; the reason being that in SiC, in contrast to Si, the carrier ionization coefficient is larger for holes than for electrons. Another drawback, which affects the IGBT Safe Operating Area

(SOA), is the presence of a parasitic npn transistor, which is more effective in SiC than in Si because of the above properties.

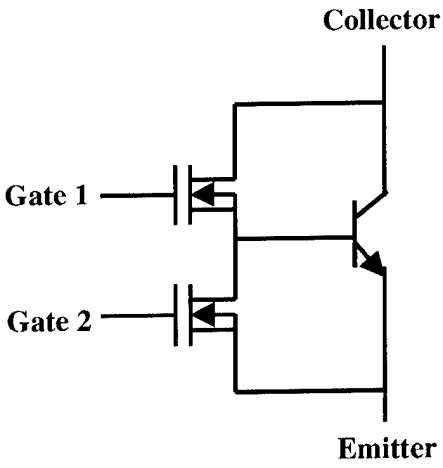


Figure 1-6. MGT equivalent circuit

These observations prompted a search for a switching device better matched to the SiC properties. This led to the MOS-Gated Bipolar Transistor (MGT). As shown in Figure 1-6, the MGT equivalent circuit consists of an integrated bipolar transistor with a floating base, which is controlled by two MOS gates, one for turning it on and the other one off. Therefore it has some similarity with the IGBT, where one MOS device controls the bipolar transistor base current. However, the MGT structure, shown in Figure 1-7, is quite different and overcomes the major drawbacks of SiC IGBTs. First of all, there is no parasitic transistor and the main bipolar transistor is of npn type, which is preferred for SiC. Second, the substrate is N+ even using NMOS gates, because the pnp transistor has been eliminated. Third, the MGT process is nearly the same as the DIMOS process. The major disadvantage is a larger cell area than an IGBT, thereby increasing the specific on-resistance lower limit for an equivalent blocking voltage, as it has been verified by modeling. As a promising device for the future and a potential replacement of GTOs, the MGT has been partially investigated in this program, although its fabrication has been affected by the same problems as the DIMOS.

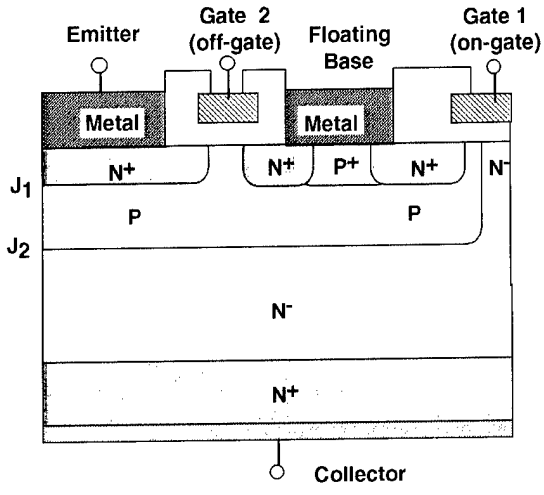


Figure 1-7. SiC MGT

Our choice of devices determined the process technology approach. To implement planar devices it was necessary to increase the knowledge of SiC implantation and annealing processes. To achieve high blocking voltage very thick (>40 μm) epi layers were needed to form the space charge region. To build GTOs with the mesa approach deep trench etching technology had to be improved to avoid micromasking defects at the bottom of the trench or roughness of the sidewalls. MOS devices required a better understanding of the MOS interface for achieving adequate mobility, threshold control and long-term gate oxide reliability. Additionally, all the devices needed the development of improved contact metallization, particularly to p-type regions. Our approach has been to subcontract these process development needs to universities already well known for their expertise and

achievements in each of these areas, while retaining the process integration and device fabrication tasks at GECRD.

Another part of the technical approach dealt with device packaging. Indeed, functional device testing and circuit assembly require packaged devices. Since the development of optimal high power SiC packaging was carried out in parallel by other programs, our packaging efforts were limited to increase the capabilities of existing high voltage high power commercial packages for meeting the program objectives. The major innovations needed were (1) SiC die bonding to replace Si dies with SiC; (2) increase of package and bonding alloy temperature up to 350 °C; (3) modification of commercial power modules to replace Si with SiC. Small companies already active in Si power device fabrication and packaging carried out all these activities under GECRD supervision. Their interest in the program and willingness to contribute were driven by the perception of the SiC technology potential and related business opportunities.

1.3. Technical Challenges

The program goals were a major stretch of the SiC power device technology as it existed at the beginning of the program. Hence it was natural to be confronted by major technical problems along the way and to have to find suitable solutions. Since these technical challenges provided a valuable learning experience, it is useful to review them here for documenting the progress made during this program.

Starting material

A key requirement for producing high-voltage (5000 V) SiC devices is the availability of thick (>30 μm), low-doped (<$2x10^{15}$ cm^{-3}) epitaxial layers. These layers must have uniform thickness and doping level, and a low defect density (< 1 def/cm^2) to obtain an acceptable yield for 200 A devices. In addition to these requirements, which are shared by both MOS and bipolar devices, a high minority carrier lifetime is necessary for bipolar devices, such as GTOs, IGBTs and MGTs, to obtain high gain and low forward voltage drop.

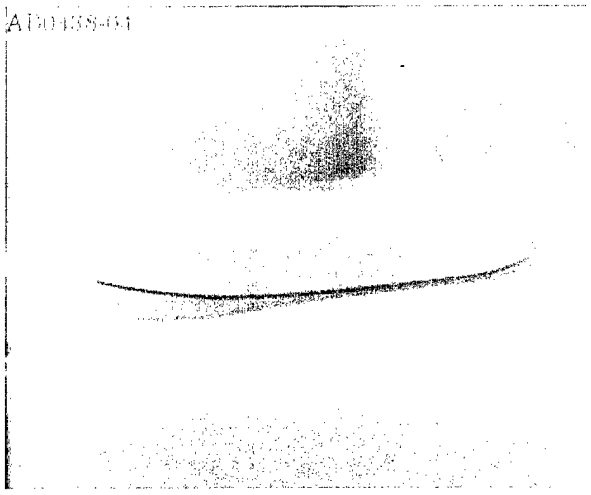


Figure 1-8. SiC wafer with large bow

The first technical challenge was to find a source of device quality wafers with one or more thick epitaxial layers. Indeed, when the proposal was submitted, a commercial source was not yet available and only Mississippi State University and NASA GRC had planned to develop this capability in support of the Megawatt SiC program. Fortunately, in the first months of the program CREE developed 10 μm-thick N-type doped epi layers on an N+

substrate. This development allowed to build high voltage PiN diodes and to relate their electrical characteristics to the epi and wafer properties.

One of the obstacles that we had to overcome was the "epi crown", which is a thick rim around the wafer edge formed during epitaxial growth. This rim can be up to 3x as thick as the epi layer and prevents close proximity of the wafer and the mask, thereby reducing pattern resolution. In cooperation with CREE a technique was developed to remove the rim with a low incidence of wafer damage, which is critical considering the cost of a SiC epi wafer.

As more complicated device structures were processed, new starting material problems quickly appeared. A most daunting one was the unacceptably large bow of 2" diameter thick epi wafers that occurred even after a simple oxidation step. Figure 1-8 demonstrates the amount of bowing by showing the shadow of the raised side of the distorted wafer as it laid on a glass surface. These wafers were unusable for device processing. Hence, we had to jointly work with CREE to resolve this problem. This type of cooperation between wafer manufacturer and user is currently sponsored by Title III mantech programs for advanced SiC wafers. GE participates in these programs by processing planar diodes for the wafer manufacturers to ensure that they meet device quality standards.

Another challenge was the sequential deposition of multiple epi layers as required for GTO fabrication using the mesa approach. The major concerns were an accurate calibration of these epi layers with regard to doping concentration and thickness and the avoidance of background autodoping from the underlying heavily doped layers. For this reason CREE was reluctant to grow a thin buffer N+ epi layer over the substrate before depositing a P buffer layer. Moreover, separate reactors were used for depositing layers with high N and P doping levels. Unfortunately, the epi stack formed in this manner exhibited a high defect density that was attributed to particle fallout during reactor change between layers. We therefore faced a dilemma. In one case, that is with the N+ buffer layer, the wafer quality was so low that we could not use these wafers for device fabrication. On the hand, when the N+ was omitted, the emitter injection efficiency of the bottom NPN transistor was very low due to NP junction formation at the substrate interface instead of between two epi layers. This problem caused significant loss of time, money and GTO performance.

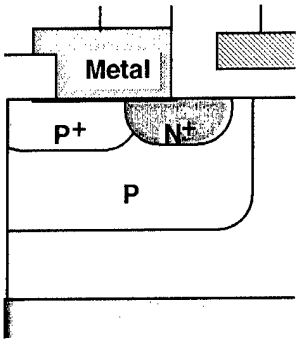


Figure 1-9. DIMOS implanted junctions

Deeply implanted regions

Planar device structures are based on sequential ion implantation of N and P dopants to form multiple stacked junctions of variable depth. In Si the ion implant range does not need to be as deep as the junction, because of a large dopant redistribution during diffusion. Instead in SiC, deep implants are needed to compensate for low dopant

diffusivity. Moreover, in high voltage devices the junction depth of a well or base region must be even higher to maintain space charge separation from an embedded region of opposite conductivity type. Figure 1-9 shows the relative position of the junctions formed by the P-base with the N- drift layer and with the N+ source in a DIMOS device. For a 5000 V DIMOS the lower PN junction must be ~2 μm deep since there is a considerable spreading of the space charge on the p-base side due to its moderate doping level. This posed a challenge, because of the unusual requirements of high-energy implants for SiC and corresponding lack of available implant facilities.

First, an implant range > 1 μm requires a MeV implanter. Second, for SiC, a heated end-station is required to keep the wafer temperature at 600 °C to 1000 °C during implant to enable adequate dopant activation during annealing. MeV machines with this capability are very rare and we had problems to find a suitable one for our experimental DIMOS run. Another problem is also the lack of adequate knowledge on deep implants in SiC despite the excellent research conducted at George Mason University under this program.

Together with our partners we made an extensive search of MeV ion implant facilites with the above characteristics. Several US universities and government laboratories have MeV accelerators, but usually their end stations are set up only for very small size samples and therefore could not accommodate full SiC wafers. For instance, this was the case at the University at Albany and Oak Ridge National Laboratory. ABB research laboratories in Vasteras, Sweden, have an MeV machine for SiC use and offered to implant samples for us as a professional courtesy. Prof. Robert Elliman of Australian National University agreed to provide an MeV implant service, but at an implant temperature of only 500 °C. Another possibility was to forgo MeV implants altogether and use instead a doubly-charged boron implant with a retrograde profile, which could be done by our normal implant service. Although the latter option was only a temporary compromise, we chose it to complete in time the DIMOS lot at a penalty of a much shorter range corresponding to 380 KeV. Therefore, we recommend for the future additional studies of MeV implants in SiC and the establishment of a domestic provider of this service.

Planar MOS structure

The development of MOS structures in SiC is a very active area of research. Its goals are to minimize interface states and fixed oxide charge, achieve an effective mobility near the bulk value, control the threshold voltage, and obtain high reliability, as measured by long-term stability of the electrical characteristics and avoidance of gate oxide rupture due to Time-Dependent Dielectric Breakdown (TDDB). These daunting requirements are further complicated in planar MOS structures formed over an implanted p-base, as needed for DIMOS, IGBT or MGT. The additional needs are (1) nearly complete activation of the p-base and (2) avoidance of surface damage during high temperature implant activation.

Activating p-type implants is more challenging than n-type, because of a higher activation temperature from 1500 °C to 1750 °C and higher dopant ionization energy,

which lowers the free carrier to acceptor ratio. On the other hand, despite its higher ionization energy, boron is preferred to aluminum for a deep implant, because of its higher penetrating power due to the small size. Hence, to meet the p-base design requirements of a DIMOS, it is necessary to achieve a high boron activation of ~50%. Consequently, the annealing temperature must be at the highest end of the above range, typically between 1650 °C and 1750 °C. The problem is that at this temperature Si vacancies are formed near the SiC surface due to Si evaporation, thereby producing surface damage, such as roughness and loss of the correct SiC stoichiometric ratio.

Many techniques have been tried to minimize Si evaporation by increasing the Si vapor pressure near the SiC surface during annealing. We routinely encapsulate the SiC wafers in a recess formed between two SiC ceramic plates during furnace annealing. This technique is adequate for lower temperature anneals, as used for n-type implants, but fails to leave a high quality smooth surface at 1700 °C. Therefore, for boron anneals a novel technique, called "silane overpressure", has been developed in Sweden at the ABB research laboratories. Our partner, Mississippi State University, has modified an epitaxial reactor to perform these anneals in presence of silane at 1700 °C or higher. Although the key objective of maintaining the SiC surface quality has been achieved, many other problems need to be solved, such as occasional wafer breakage caused by thermal gradients during heating and cooling.

We believe that the silane overpressure technique is necessary for activating the p-base implants and creating an MOS-quality surface for device fabrication. However, until the ancillary problems associated with this technique are eliminated in a reliable commercially available production equipment, its use will be very limited due to the danger of loosing partially processed wafers. This is a challenge that needs to be addressed to approach the development of planar ion-implanted MOS-gated power devices.

1.4. Program Execution

This program consisted of three main development activities: (1) process technology; (2) device development; (3) circuit analysis. The program ended with a transition phase to transfer the results to GE businesses and industrial partners for defense and commercial applications. Figure 1-10 shows a block diagram of the program workflow and the contribution of various team members.

Process Technology

At the beginning of the program GE had already accumulated a large experience in SiC device processing with significant achievements, including the first monolithic SiC operational amplifier and the first SiC IGBT. These techniques, equipment, personnel and facilities were utilized in this program providing a valuable continuity and a jump-start. Nevertheless, the novel SiC power devices designed for this program required the development of advanced SiC process technology.

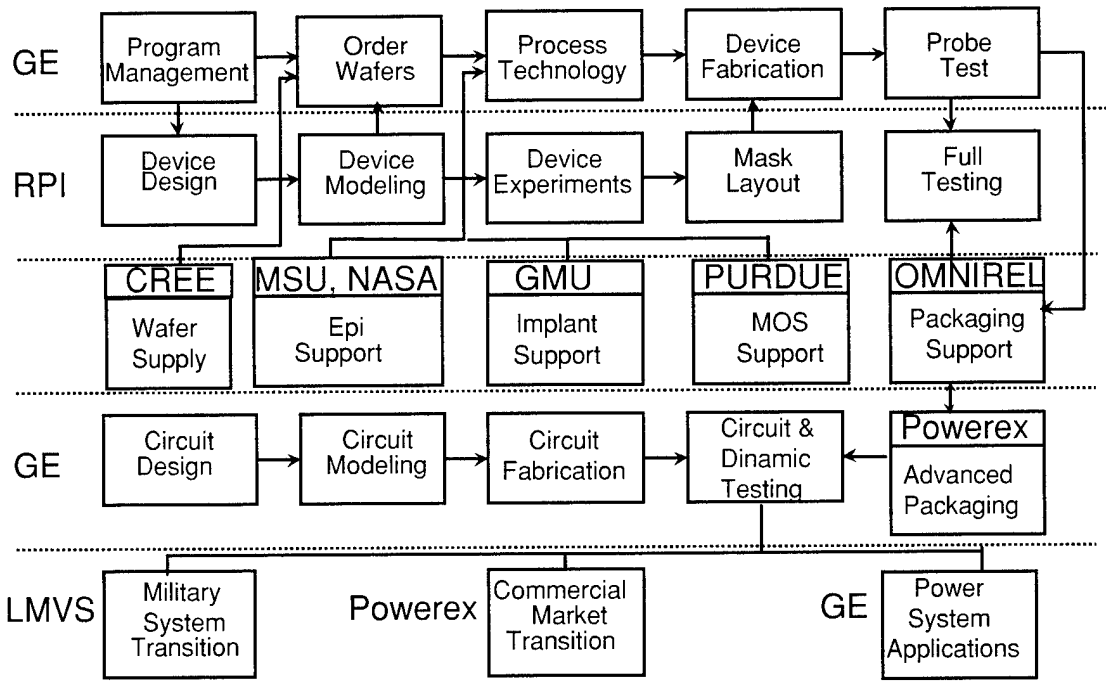


Figure 1-10. Program workflow

We chose to reserve for GE the process integration task while utilizing the support of various universities and organizations for specific process technology tasks. Our major concern was to optimize the task distribution on the basis of our evaluation of the most suitable task holder, based on subject experience, technical leadership, synergy with other programs and probability of success. For instance, since RPI had a MURI program in SiC power devices, a preliminary feasibility demonstration of new devices could be carried out under the MURI program thereby reducing the processing risk under this program. Similar synergy existed with regard to MSU and NASA Glen support for thick epitaxial growth, GMU for deep ion implantation, and Purdue for MOS gate oxide formation.

Another characteristic of our working relationship with our partners was the use of lot splits to compare baseline processes with novel process technology steps just developed by the partners. This research mode was mutually advantageous, because GE did not have to set up new equipment with considerable time and cost investment, while the partner had the opportunity of determining the device effect of these steps. Moreover, it provided a systematic method of making engineering upgrades to the baseline process with a rapid insertion of novel processing techniques. Specifically, this activity was very effective for the evaluation of boron implant annealing methods and various methods of gate oxide formation.

The process technology phase ran in parallel with new device development, always preceding the corresponding device fabrication. Therefore, the issues addressed at first were those of interest to all high-power high-voltage SiC devices, such as thick epi, wafer

quality acceptance, low contact resistance, and boron/aluminum implant annealing. As GTOs were ready for processing, deep SiC trench etching and multiple epi layer formation became major development items. Finally, for DIMOS and MGT fabrication it was necessary to generate a viable MOS process flow for planar power devices. Technical details of these developments are described in later chapters.

Device Development

The device development activity was mainly performed be GE and RPI. As seen in Figure 1-10, RPI designed the devices along GE's specifications, performed the numerical 2-D modeling, generated the wafer specifications, laid out the masks, conducted experiments to verify the process feasibility, and functionally tested a portion of the dies. On the other hand, GE ordered the wafers and the masks, added the GE process test vehicle, processed the devices, tested the devices at the probe station, and functionally tested a group of dies for circuit parameter extraction. In addition, GE and RPI mutually supported each other in terms of processing equipment to keep the lots on schedule during equipment downtime.

CREE also played a major role during device development by supplying wafers with novel specifications not yet included in the catalog. This allowed implementing innovative device designs, which in turn produced new records for key device characteristics. For instance, CREE delivered 70 µm thick N-type low-doped epi, which made possible the fabrication of ion-implanted PiN diodes with >5000 V blocking voltage at a yield >50%.

An important aspect of the device development phase was the choice of schedule and the distribution of work. Since the development tasks are the same for all the devices, i.e. design, modeling, layout, fabrication, etc., we decided that a pipeline approach was most useful to make the best use of resources and avoid bottlenecks. Hence, each device development started sequentially with simpler devices preceding the most complicated one or those waiting for a scientific breakthrough, such as the planar MOS devices. Every device was the responsibility of a different PhD student of Prof. T.P. Chow and was the subject of his PhD thesis. This ensured a complete dedication from the student to generate high quality publishable results and identified to the team a unique knowledge source for each device.

After the first round of experimental device lots, additional lots were processed either to supply new devices for circuit use or packaging, or to optimize the choice of device parameters according to the test results. A device lot rerun after a long time interval is also important for leveraging wafer quality improvements, such a lower defect density, higher doping accuracy, or a thicker epi layer. All these parameters have a major effect on the device characteristics.

This program did not include an advanced packaging development task, but relied on adapting commercial Si packages for use with SiC dies. Hence, a minimal effort was employed to select the packages and learn the techniques for die and wire bonding SiC

chips using brazing alloys with high eutectic point above 350 °C. Omnirel, Leominster, MA, successfully packaged the SiC devices for functional testing and later insertion in a circuit board. In parallel, the hybrid facility of Lockheed Martin Control Systems, Fort Wayne, IN, provided a similar service using packages fabricated by a specialty supplier, Sinclair Manufacturing Company. This company spent internal funds to develop a package that would withstand 5000 V, 100 A at 350 °C to prevent derating of our SiC 5000 V devices after packaging.

Circuit Analysis

Modern power circuit methodology requires circuit and system modeling before circuit fabrication to avoid unnecessary hardware iterations. Therefore, an important task was the generation of SiC device models for use in a commercial power circuit simulator, such as SABRE by Analogy, Inc. For this reason, static and transient device characteristics had to be measured to extract the device parameters for the simulator.

The unusual characteristics of SiC devices, especially the combination of high voltage and fast switching performance, required the design and fabrication of special test circuits. Since these were not commercially available, GE invested considerable effort in this activity and used these tools to measure not only the in-house produced SiC devices, but also those from other teams of the SiC community. To ensure a fair comparison, the GE team also procured and measured Si devices, which best matched the SiC characteristics. This produced the information necessary to identify and optimize various power circuit applications without restricting to a single semiconductor choice.

On the basis of the current level of technology readiness, the most promising early applications were those utilizing a half-bridge inverter with Si IGBTs and SiC diodes. The key advantages were fast switching characteristics and lower power dissipation not only of the SiC diodes, but also of the Si IGBTs. Because of the importance of this building block circuit, already recognized in the proposal, GE and Powerex developed a packaged module containing a matched pair of these devices. This has been fully characterized and could lead to a possible product, since it will be a pin-compatible upgrade for existing power systems.

1.5. Technical Achievements

Several important technical results were achieved along the course of the program. Although their technical discussion will follow later, we present here a summary of these achievements to provide an overview of our technical progress and recognize its impact on SiC technology development in general over the last few years.

Switching behavior of high voltage SiC PiN and Schottky diodes

When the program started a major gap existed between the ambitious goal of seeking megawatt power device rating and the inadequacy of typical device characterization even for modest power device applications. The reason was that devices were usually

characterized by their developers, whose main interest was to optimize the device design and process technology. Therefore, electrical testing usually consisted of measuring static I-V and C-V characteristics. Hence, application engineers and power system designers lacked those parameters, which were most meaningful for predicting device behavior in a circuit, especially under transient conditions. Our team addressed this issue.

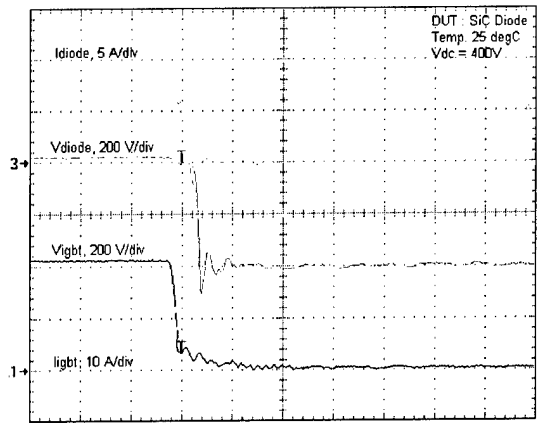


Figure 1-11. Voltage and Current Waveforms at 25°C when a SiC Diode is used as DUT. Scale=50ns/div, di/dt=480A/μs

We conducted a systematic investigation of the switching characteristics of junction and Schottky diodes to measure dynamic parameters, such as reverse recovery time, t_{rr}, reverse recovery current, I_{rr}, turn-on time, t_{on}, and maximum dI/dt. These parameters were measured as a function of temperature and compared with those of fast recovery Si and GaAs diodes. Figure 1-11 shows a typical oscilloscopic trace of SiC PiN diodes. These results were published in Solid-State Electronics, Technical Digest of IEEE Industrial Application Society and Proceedings of the 3rd All-Electric Combat Vehicle conference.

The findings of this investigation confirmed the theoretical expectations. The reverse recovery current, I_{rr}, and reverse recovery time, t_{rr}, are about 10x smaller for SiC diodes than for equivalent Si diodes. This ratio increases with temperature, as observed comparing measurements at 25 °C vs 150 °C. Consequently, the switching energy for a circuit employing SiC diodes is significantly reduced, thereby allowing operation at higher frequency with lower power dissipation and reduced thermal sink. This feature is a compelling reason for using SiC diodes in many applications, either with SiC or Si switches.

SiC GTOs with involute and concentric gate pattern

Retracing the evolution of Si power devices, SiC SCRs were among the first bipolar switches to be implemented in SiC technology. Although designed on very small chips with single cell layout, these early prototypes demonstrated high frequency switching and superior current density compared to Si. We went a step further by investigating a highly interdigitated GTO, that is a multiple cell SCR with many design and processing variants to optimize the gate geometry and the junction termination. This marked the transition from a device physics objective to a device engineering goal with opportunity for scaling to larger dies as the material quality improves.

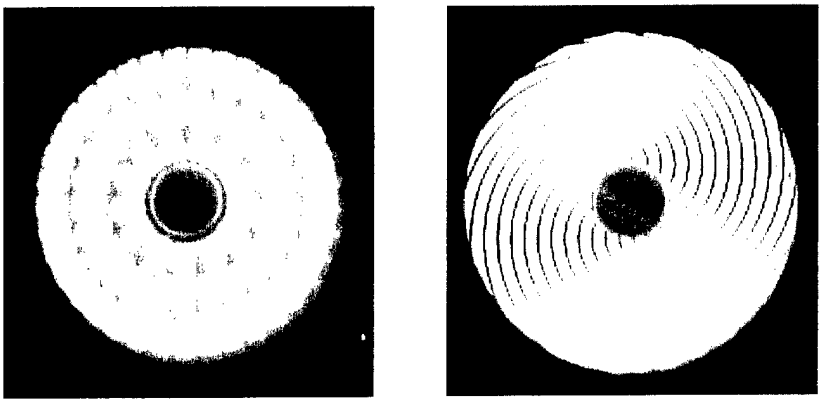
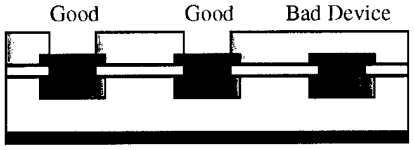


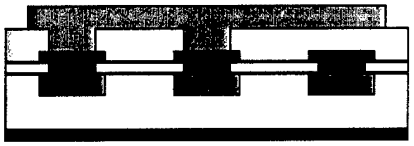
Figure 1-12. SiC GTOs with Concentric and Involute Geometry

SiC GTOs with a 3-ring junction termination extension (JTE) were designed for 5000 V blocking voltage. A parametric mask layout allowed to evaluate several design variants. The GTO cells measured 800 μm, 1200 μm and 2400 μm, and were of two types: Involute and Concentric, as shown in Figure 1-12. The anode width measured 20 μm, 40 μm or 80 μm to evaluate its effect on GTO turn-on and turn-off time.

1. Device (e.g. diode, GTO) fabrication
2. Full wafer testing
3. Mapping of functional sites



4. Open vias only to good devices using laser selective writing



5. Deposit a thick metal layer for Wire bonding

Figure 1-13. SiC diode interconnection process

The GTO structure consisted of 4 epi layers on a 4H-SiC N+ substrate. Cree supplied the wafers according to GE and RPI specifications, which were optimized using the MEDICI simulator. The measured blocking voltage was > 1000 V at 25 °C. The forward drop, V_f, was 5 V at 100 A/cm^2. At 190 °C, the turn-on time was 0.7 μs and the turn-off time 2.0 μs, thereby confirming the high speed switching of these devices. Two GTO lots were processed providing a range of process and design parameters, whose effect on the device electrical characteristics was the subject of a PhD thesis at RPI.

Wafer level diode multiplexing

Present SiC power devices, even as simple as diodes, are current-limited by the SiC material quality, which limits the die size on the basis of an acceptable yield. This is a stumbling block for many SiC applications, because of higher current rating of competing Si devices. Hence, there is a great interest in techniques that would provide SiC diode multiplexing with minimal process complexity. We

explored one of these techniques using a wafer level parallel interconnection of proven good dies.

Our process consisted of connecting with a metal plate groups of 4 or 16 adjacent good diodes, which were pre-tested on a wafer probe station. The process flow is shown in Figure 1-13. Vias were opened through a thick passivation layer only to selected "good" dies using laser direct-writing. Bonding pads were then formed as usual over the final metallization.

This technique was partially successful and requires further investigation. The forward characteristics exhibited the expected current increase, but the blocking voltage was reduced in comparison to the original value. We believe that the dielectric strength of our passivation layer was inadequate for 5000 V electrical isolation. In the diode off-state this voltage must be supported by the passivation layer when the anode metal plate crosses over a failed diode or over the separation region between adjacent diodes, which are at cathode potential. The addition of a thick polyimide layer to the original silicon oxide passivation may solve this problem and could be an interesting experiment for future programs.

SiC CVD epitaxy and silane overpressure annealing at MSU

When the program started, a source of thick low-doped N-type SiC CVD epitaxy was desperately needed for achieving the program objective of developing devices with blocking voltage > 5000 V. At that time CREE was not yet ready to supply these wafers and NASA Glen was involved with the installation of two new commercial reactors. Our partner, MSU, came to the rescue with NASA support by upgrading a CVD epi reactor and outfitting it with a 75 mm diameter tube. This change allowed epi growth on 2" (50 mm) diameter wafers, thereby complying with CREE's plans for a substrate diameter increase. Figure 1-14 shows a picture of the new MSU epi reactor.

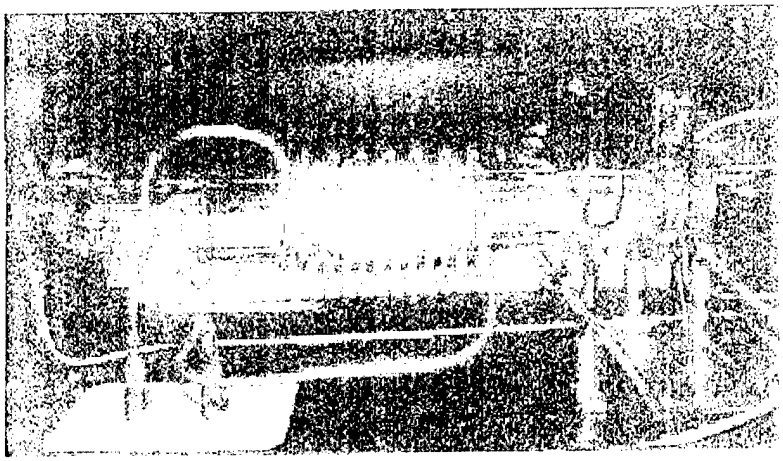


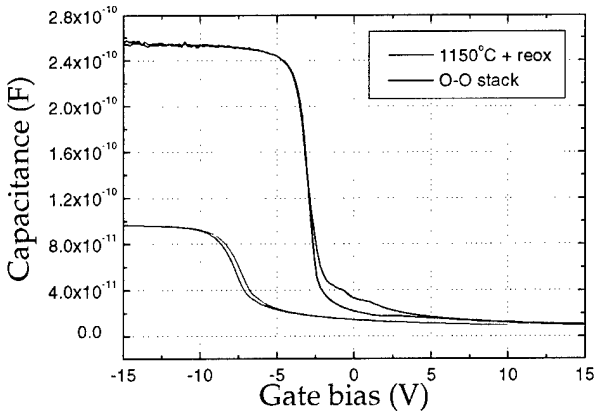
Figure 1-14. SiC 75 mm-diameter MSU epi reactor

In addition to the growth of thick low-doped N-type epi for high voltage diodes, the MSU team also developed thick p-doped epi layers to form the drift region of GTOs in response to this program needs. For the same reason, heavily doped P+ layers were developed to form low contact resistance ohmic contacts to the GTO anode.
The same reactor was also used for developing a silane overpressure process for annealing implanted wafers in cooperation with GE, ABB and Purdue University. The silane overpressure technique is a promising technology to reduce the surface damage during high temperature annealing. This requirement is particularly important for MOS oxide growth that depends on good SiC surface properties for minimizing interface states and achieving an acceptable channel mobility.

Evaluation of gate oxidation techniques at Purdue University

GECRD's techniques for SiC gate and field oxidation evolved from the development of signal MOSFETs for high temperature sensor applications. In view of recent gate oxide advances, these techniques had to be reassessed and optimized for use on fully-implanted vertical power devices with planar MOS input gates, as required by this program.
This task was assigned to Prof. Mike Capano of Purdue University, because of the leading research conducted in this field at this university. These methods were: (1) Steam oxidation at 1050 °C and 1100 °C; (2) Steam oxidation plus 950 °C reox anneal; (3) High Temperature Oxide (HTO) deposition at 900 °C with and without reox anneal. These studies included both n- and p-type SiC, mostly 4H, with few 6H samples for comparison.

The GECRD technique of HTO deposition followed by 950 °C reox yielded the best results, as judged by the small flatband shift (Vfb=-3.6 V on p-type SiC), low interface states density (Dit <1e12cm-2 eV-1) and slow oxide traps. Figure 1-15 shows the C-V curves comparing the single oxide versus the GECRD double oxide (O-O) stack. Based



Flat band shifts:

-8.2 V w/ reox

- 3.2 V w/ reox

Figure 1-15. C-V curves of single vs thermal+deposited (O-O) oxide stack

on these results, a preferred gate oxidation technique was formulated for DIMOS, which consists of a plasma and RCA cleaning, a thin steam thermal oxidation at 1050 °C to form the interface, an HTO oxide deposition at 900 °C to reach the desired film

thickness, and a reox anneal at 950 °C. Despite the good performance of this technique, the problem of gate oxide formation on an implanted p-base has not been solved and negatively affected our DIMOS lot.

DIMOS process development

As widely reported at technical conferences and in the literature, it was clear from the start that the development of DIMOS devices was going to lag compared to GTOs and other bipolar devices. Nevertheless, it was necessary to run full DIMOS lots in order to test the progress made in specific areas of process technology and to provide feedback to the researchers.

Our previous experience with SiC mesa MOS power devices and IGBTs led us to select the fully implanted planar approach. We use lot splits to evaluate variants of ion implantation and annealing for the JTE, p-base and n+ regions. Moreover, we evaluated various gate oxidation methods to improve the MOS channel performance.

We conducted several annealing experiments in cooperation with Mississippi State University using a silane overpressure process developed there. Additional experiments were also planned for MeV p-base implants, but time constraints and lack of suitable facilities made us settle for a double-ionization boron implant with a reduced depth range.

JTE-terminated fully-implanted SiC PiN diodes with BV > 6KV and yield > 50%

Our initial PiN diode design was based on the program electrical specifications with the customary 10% margin. Hence, the thickness and doping of the epi layer were selected for a blocking voltage, BV, slightly above 5000 V. This led to the choice of a 40 μm-thick epi for the first lot. However, the measured PiN diodes exhibited low yield, not so much because of shorts, but because of low blocking voltage. The problem was ascribed to small surface defects, which caused premature junction breakdown.

Fortuitously, at that time, Lockheed Martin Fire Control Systems (LMFCS), Dallas, TX gave to GECRD the task of investigating new power electronic technology for an electromagnetic (EM) gun launcher. With LMFCS funding we designed and fabricated a lot of SiC PiN diodes on 70 μm-thick epi to achieve a blocking voltage, BV > 10 KV.

The PiN diodes were fully implanted with a 3-ring JTE termination. We found that on one wafer the 800 μm x 800 μm diodes exhibited BV > 6KV with 50% yield, as shown in Figure 1-16. The leakage current at 6 KV was <20 μA, that is 3 mA/cm2, and in another wafer it was as low as 0.7 μA at 5 KV, that is 0.1 mA/cm2. The forward drop was 5.5 V at 200 mA and 10 V at 1 A. On one wafer the 4 mm x 4 mm diodes were functional with BV of 2-5 KV and forward current of 10 A at 10 V. The major failure mechanism was a catastrophic short occurring frequently during testing despite protection of the surface with fluorinert. This led to the conclusion that the diode passivation was inadequate for such a high voltage causing its early breakdown.

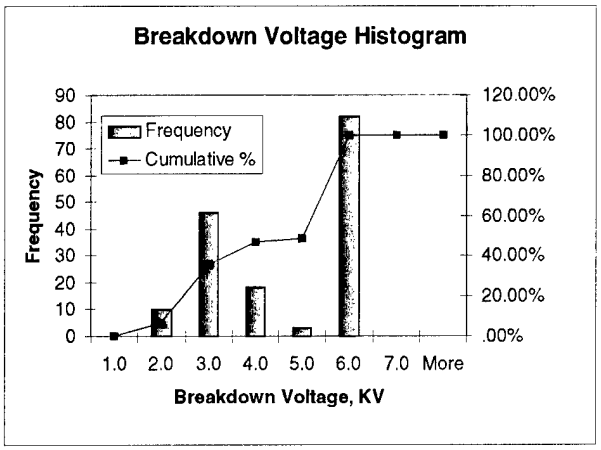


Figure 1-16. Breakdown voltage histogram of PiN SiC diodes on 70 µm-thick epi

The important lesson obtained from this lot was the discovery of a simple technique to increase the parametric device yield with state-of-the-art SiC wafers. By overspecifying the epi thickness and increasing the edge width around the device perimeter one can shift the blocking voltage distribution toward higher values and therefore place most of the distribution above the BV specification. This technique also provided a satisfactory yield of larger area diodes (4 mm x 4 mm) with a correspondingly higher current rating. The advantages by far overshadow the higher cost of the thick epi and the increase of drift resistance caused by the thicker epi.

Hybrid SiC/Si half-bridge inverter module

A main goal of this program has been the insertion of SiC power electronic components into circuits. A determinant factor is the external configuration of these components. Obviously, a similarity of packaging and functionality with equivalent Si components will be a big incentive for accelerating the introduction of the new technology.

Figure 1-17. Hybrid Si/SiC half-bridge inverter module

On these premises, we teamed with Powerex, Youngwood, PA, which is a major producer of high power devices and intelligent power modules, to modify a half-bridge inverter module by replacing the Si diodes with our SiC ones while retaining the Si IGBTs. Since the package is the same, a one-to-one module replacement is possible without the cost of circuit board changes. Hence, this development has the potential of becoming a product. Its use will be economically justified in those applications, which can afford a higher component cost to achieve the performance advantage of SiC.

The module consists of a Si IGBT cascaded with a flyback PiN diode. This is a basic building block for motor drives, power supplies and many other power circuits. Its construction and electrical characterization will be discussed in detail later. Figure 1-17 shows a picture of this module, which has the same external appearance of a commercially available all-Si part. By providing this module with a catalog-type data set an application engineer will have all the technical elements for utilizing this part in his designs. The insertion then becomes a matter of cost and volume supply, which depend on the emergence of SiC power device manufacturers as the technology matures.

1.6. Transition

We believe that technology transfer is a key factor to measure the success of a program. Therefore, in our plans we matched SiC power device development with functional testing and application analysis. Furthermore, to ensure acceptance of the test results by system designers, we assigned these tasks to them and let them choose their own metrics and methodology. These are the same designers, who are responsible for short-term power electronic innovations at GE businesses using commercially available Si

Table 1-3. SiC power device applications

Commercial & Industrial			Defense		
Application	System	User	Application	System	User
Traction Inverters	Locomotives	GE Transport. Systems	EM Gun	Combat Vehicles	LM Fire Control Systems
Industrial Drives	Factory Automation	GE Industrial Systems	Switching Power Supplies	Satellites and missiles	LM Space Systems
X-ray Generators	Medical Diagnostics	GE Medical Systems	EM Actuators	Aircraft Controls	LM Aeronautical Systems
Utility Power Conditioners	Electrical Distribution Network	GE Power Systems			
Megawatt Power Converters	Power Conversion Stations	GE Power Systems			

components. In this way, the gap between long-term R&D and current problem solving has been reduced resulting in an accelerated technology transition.

The main technology transfer achievements of this program are:

1. Comparison of SiC and Si power devices on test circuits and assessment of the best utilization conditions for both technologies.
2. Generation of circuit analysis models for SiC power devices using commercial power system simulators, such as SABRE (Analogy, Inc.). This is a prerequisite for designers to seriously consider new components.
3. Interactive feedback from circuit designers to SiC device developers and packaging engineers.
4. Listing of potential applications for SiC power devices. For each application we established the rating requirements, utilization mode, i.e. either SiC alone or mixed with Si, application sector, i.e. industrial, commercial or defense, and approximate SiC technology maturity level.
5. First-hand knowledge of SiC power device capabilities, electrical data and device sources among key designers. In due time this will lead to successful applications since this knowledge will be available to leverage opportunities and for problem solving in the field.
6. Many talks on SiC applications to industrial technology forums, such as IAS (IEEE Industrial Applications Society), and to defense conferences, such as AECV (All Electric Combat Vehicles).
7. Establishment of a functional device testing service at GECRD. This allows producers of SiC power devices to get an objective evaluation of their prototypes and indirectly obtain exposure of their future products to a prominent industrial company, like GE.

Table 1-3 lists promising SiC power device applications for civilian and defense use at GE and Lockheed Martin (LM). The identification of these opportunities is only a first step toward their implementation. At present a major obstacle is the lack of SiC power devices on the market. Only CREE and Infineon are supplying evaluation prototypes, but without a firm price or production date. Therefore, lacking these critical decision elements, the business units at GE and LM can only engage in prototype design and engineering of SiC-based power systems.

Moreover, the level of technology readiness depends on the power device type being inversely proportional to its complexity. This suggests that early SiC applications will use simple diodes, whose availability and reliability will occur first. Later applications will progressively incorporate more complex devices, such as GTO and gate-controlled switches. The experience acquired by our system designers using devices fabricated during this program has provided a significant step forward on the learning curve, satisfying a major objective of the technology transition task.

1.7. Publications

The technical knowledge developed during this program was shared at first with the SiC DARPA community and later published in conference proceedings and technical journals by the team members. This activity is still in process as additional articles are being submitted for a later publication date.

Our sponsors have always encouraged this information exchange to accelerate SiC technology development and provide a forum for discussion of technical achievements versus users needs. Specifically, by publication of early device results, this program contributed to defining a trend of SiC high-power high-voltage devices for inclusion in a power electronics roadmap. This is important for system designers and technology planners to coordinate the insertion of SiC technology, generate the necessary infrastructure, and ensure an economically sustainable growth without direct government support.

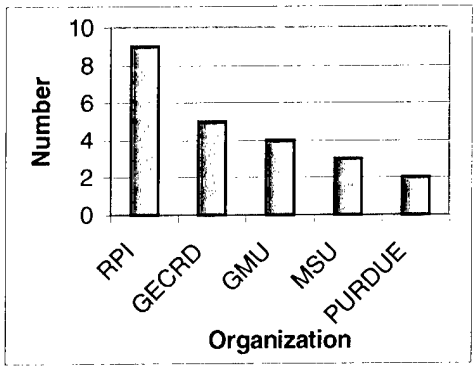


Figure 1-18. Publication source

Another form of technology dissemination is by Ph.D. thesis. In fact, the competence acquired by a graduate student while conducting research on a new technology is an excellent mean of technology transfer to his future employer. Many graduate students at leading US universities, now employed in industry, have used this program to conduct research for their thesis. Their direct involvement with SiC power devices will allow them to monitor the progress of this technology and thus suggest a suitable entry of their companies into this arena.

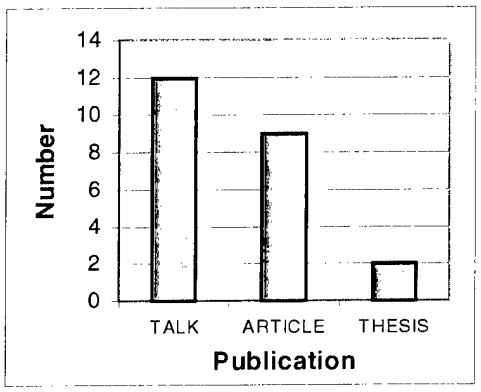


Figure 1-19. Publication type

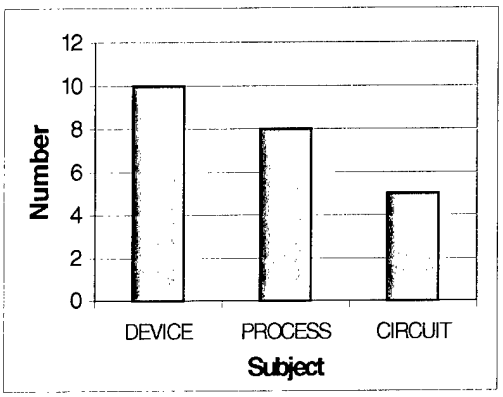


Figure 1-20. Publication subject

As customary, publications are referenced at the appropriate text site of this report. Hence, to avoid duplication, we will not list here all the publications produced during this program, but will analyze their origin (Figure 1-18), type (Figure 1-19) and subject (Figure 1-20) based on information available at the time of writing. For this reason, we

apologize to the authors if this analysis does not include all their articles and publications and for any discrepancy between these data and those of the publications list provided by the authors, which is included in the appropriate chapter. It is also likely that additional articles sponsored by this program will have been published in the meanwhile, because of the time delay between research performance and publication.

As expected there were more oral presentations than articles, because (1) talks are a mean of communicating research in progress, and (2) articles are published as much as a year after submission. For a similar reason we counted only two Ph.D. theses, because of even longer interval from the candidacy exam to the thesis defense and publication.

RPI generated the largest amount of publications, because it was the main subcontractor and performed research on the key program topic, i.e. SiC power device technology. This explanation is also confirmed by the fact that the classification by subject shows a predominance of device publications. Instead, the number of process technology publications for each university subcontractor closely matched the corresponding participation to the program.

GECRD generated all the publications related to circuits and applications. This role was extremely important to the program success, because it brought the technical results to the attention of the users with the awareness of their needs and their concerns for this technology. Moreover, because of GE's prominent role as an electrical system manufacturer, these publications conveyed an objective assessment of opportunities for SiC power electronics and a vision of potential applications as the technology matures.

2. Process Technology

The SiC Megawatt program fostered advances of SiC process technology that enabled the development of novel power device structures and improved key electrical parameters such as contact resistance.

The process technology needs were identified at the beginning of the program according to the proposed process flow for various devices. This allowed an early start of the process technology development task and yielded, whenever feasible, timely results for use in device fabrication. Unfortunately, there were cases where the needs could not be satisfied during the program despite our efforts and those of the entire SiC community. For instance, the problem of developing a high quality MOS gate dielectric with low interface states is still eluding the research community and will probably be an obstacle for SiC MOSFETs for many more years.

As mentioned earlier, our approach to SiC process technology development has been to assign various subtasks to leading experts in each topic, since they already have a large knowledge base, the appropriate equipment, the scientific network in the field, and the interest to continue and excel in this work. Therefore, subcontracts were stipulated with leading universities with a demonstrated record of achievement in each field and a commitment to technology transfer through publications and other forms of technology dissemination. The adherence to these principles is evident in the brief synopsis of this chapter, whose subject discussion follows the same order as the process flow.

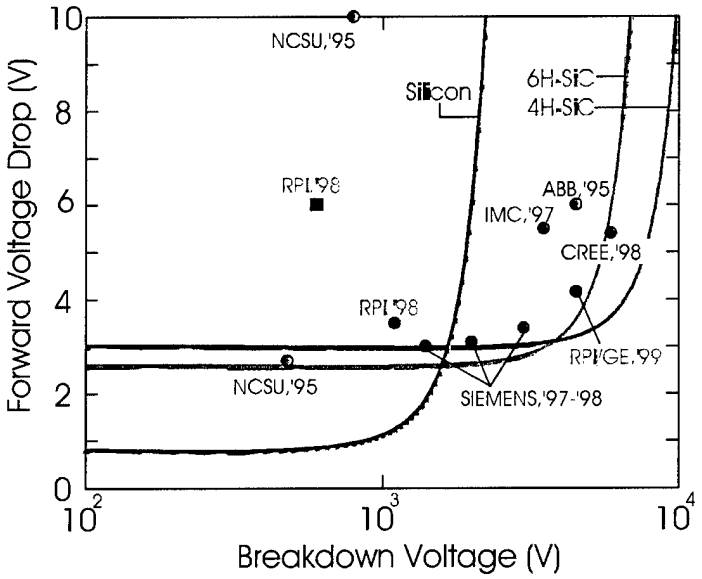


Figure 2-1. Advanced SiC diode technology map

SiC epitaxy of thick layers with very low doping is necessary to form high voltage power devices, as required by the program. Profs. Stephen Saddow and Michael Mazzola of Mississippi State University, Emerging Materials Research Laboratory, have been the

principal investigators of this task. Their research allowed us to design our devices with confidence using stretched specifications for the epi wafers. Although the wafers were purchased from CREE for practical reasons, the combined support of MSU and CREE led us to produce in 1999 fully implanted PiN diodes with record high breakdown voltage. Figure 2-1 shows the key parameters of GE/RPI diodes made during this program compared to other results. It is remarkable that these diodes have one of the lowest forward voltage to breakdown voltage ratio despite the exclusive use of ion implantation for their fabrication instead of multiple epi layers.

SiC trench etching is needed to form the GTO mesa structure. A common problem is the formation of "stalagmites" or "grass" at the bottom of the trench, as a consequence of micromasking by metal particles. Several etching techniques were tried at GECRD using various masking layers stacks and etching chamber configurations. Close cooperation with the team of Prof. T.P. Chow of Rensselaer Polytechnic Institute allowed to exchange etching technology information and samples to optimize the technique. However, we found that there is only a narrow safety margin for etching perfect trenches, because the techniques that eliminate micromasking are susceptible to other etching problems, such as the formation of thin wall residues near the edges of the trench. Fortunately, their effect on GTO performance has been limited and was secondary compared to more pressing problems, such as doping concentration and lifetime control of critical regions.

Our program used ion implantation more extensively than in earlier SiC devices, because of its potential to yield selective and accurate doping control without loss of surface planarity. However, this technique was not yet mature in SiC and therefore we subcontracted Prof. Mulpuri Rao of George Mason University to advance the scientific knowledge in this field. Our aim was to use the results of these experiments for defining suitable implant conditions for our devices. Of special interest were the choice of dopant species to lower the sheet resistance of implanted regions and the studies of deep ion implantation for implementing planar DIMOS structures.

Although our primary focus was the development of bipolar diodes and GTOs, we also had the objective of exploring MOS power devices. Since we were well-aware of the problems associated with the gate dielectric in SiC, we subcontracted these studies to Prof. Michael Capano of Purdue University, because of the excellence of this organization in this field. The goal was to compare GECRD technique of gate dielectric formation with the best techniques developed elsewhere differentiating among substrate type, doping conditions and annealing treatments. This was a focused effort aimed at defining experimentally the most favorable gate dielectric formation method for our DIMOS process sequence.

One of the major processing challenges in SiC is the annealing treatment for p-type implants. The dilemma is the choice of a suitable temperature and annealing conditions that would achieve nearly complete activation with minimum Si evaporation and associated surface damage. Prof. Stephen Saddow of Mississippi State University replicated in his laboratory a successful annealing technique originated at ABB Research Laboratories, Vasteras, Sweden. This offered us the opportunity of comparing our

furnace annealing technique with the novel technique, called "silane overpressure". The results were very encouraging, but a commercial apparatus is needed to apply with confidence this technique to device wafers, since the temperature gradients during annealing can cause wafer breakage in a laboratory apparatus.

Contact resistance is a major component of the forward resistance of power devices and must be minimized to reduce power dissipation. The problem is particularly severe for contacts to p-type regions, because of the reduced acceptor concentration and consequently higher Schottky barrier. The contact resistance is affected by the choice of contact metal stack, contact annealing, and SiC doping technique, either by epi layer doping or ion implantation. We evaluated in a factorial experiment all the combinations of these variants that were considered promising at the beginning of the program. The results suggested that Al/C ion implantation with an Al/Ti metal stack is a good choice for making p-type contacts with low contact resistance. Hence, this technique was used for the standard process flow during the entire program.

The choice of final passivation is important for high voltage power devices, because adjacent surface regions of PiN structures must support the full blocking voltage. While the junction termination extension reduces the electric field within the SiC, the passivation must provide similar protection against catastrophic breakdown in the upper dielectric structure. Unfortunately, this portion of process technology is not receiving the attention that it deserves until the devices are transitioning to production. We are also guilty of the same fault and our efforts have been limited to identifying the problem, but were weak in finding a solution. Nevertheless, we will present our failure analysis and our suggestions to eliminate this problem using experience accumulated in Si power device development.

2.1. Epitaxy

2.1.1. Epitaxial Layers for High-Voltage Devices

The goal of this research was to develop all of the necessary equipment to grow repeatable, high quality epitaxial device layers by means of CVD in a 75mm-diameter reactor. With the largest diameter wafers commercially available being 2", this SiC CVD reactor is adequately equipped for future substrates. Typically, a 50 μm epi layer of $1x10^{15}$ cm^{-3} net doping density can block 5,000 volts, which is desirable for many electric vehicle and power conditioning applications. As a consequence, the direction of this work was along the lines of not only increasing the quality of conventional epi layers on large-diameter (2" or greater) SiC substrates, but also in increasing the growth rate to deposit in a reasonable time epi layers of about 50 μm.

2.1.2. Epitaxial Layer Performance Requirements

In addition to the obvious need for lightly doped, thick epitaxial layers for power switching applications, the need for epi with low defect density is clear. These defects may be either crystallographic (dislocations, micropipes, etc) or electronic (point

defects). Conventional wisdom is that epi is only as good as the starting substrate material, which is in general true. However, if great care is made to purify the epi growth process, then a significant reduction in point defects is typically achieved. However, it is not typical that crystallographic defects are reduced during epi growth, although some defect annihilation may take place and it is well known that micropipes are reduced in diameter but never eliminated completely. In this program epi growth on reduced micropipe density substrates was performed to assess the suitability of this approach to reducing crystallographic defects in the epi originated in the substrate material. A three-fold increase in breakdown voltage of Schottky diodes was achieved early on, but confirmation of these results is still pending. The results of this work, plus the main epitaxy goals of thick, low-doped, high-quality epi are discussed next, starting with the status of epi growth in the Emerging Materials Research Laboratory (EMRL) at Mississippi State University at the beginning of the program in 1998.

2.1.3. Status of Epitaxy at Program Start

At program start, technology experiments were conducted with the aim of demonstrating device-grade epitaxial layers meeting GECRD device design requirements. This involved the establishment of repeatable doping concentrations from 1E15 cm^{-3} to 1E19 cm^{-3} of both n- and p-type polarity. Initial technology demonstrations were carried out in the 35 mm cold-wall system, and solid progress towards meeting the device goals of low-doped, thick epitaxial layers was made. One of the prime GECRD epi specification requests was the establishment of n–type layers in the doping range of 1-3E15 cm^{-3}. This was achieved for epi thickness of up to 10 μm, as determined by C-V measurements, in both the 35 and 75 mm CVD systems. This background doping concentration has been repeated several times, indicating the establishment at EMRL of a reliable process for this critical device layer. Figure 2-2 shows a doping matrix for the 35 mm tube at the start of the program.

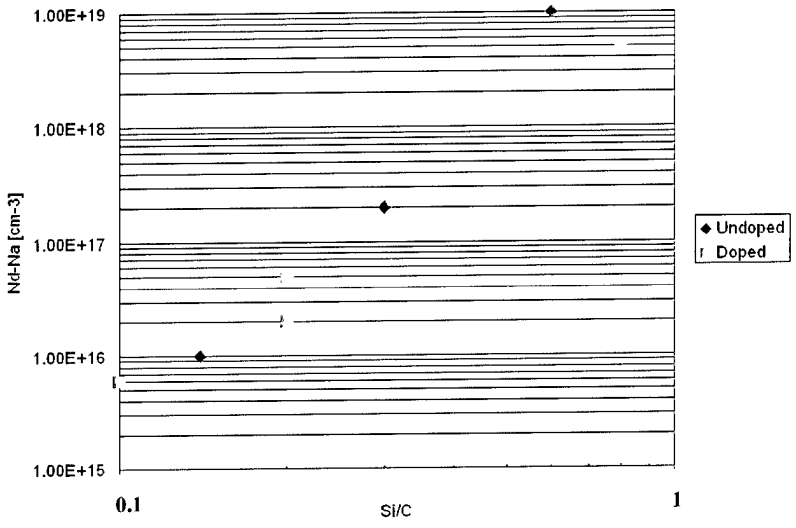


Figure 2-2. Doping density versus Si/C for EMRL's original 35mm cold-wall CVD reactor [2]. Doping density measured via Hg-probe C-V in EMRL.

During doping characterization of the 35 mm reactor a low-doped p-type epi layer was grown on a GE supplied substrate. The goal was to achieve a p-type doping as light as possible. Unfortunately, because of our nitrogen-dominated reactor, the C-V measurement of the epi layer did not show the expected type conversion. In preparation for the C-V analysis, GE deposited a layer of SiO_2 over the whole wafer supplied by EMRL and then formed metal contacts to permit MIS capacitor characterization of the epi layer. GE data defined this layer as a low-doped n-type 6H-SiC material with a net background doping concentration in the 1-3E14 cm^{-3} range. It was later discovered that some of the epitaxial layer material was n-type, and some p-type. Clearly a more repeatable method of achieving p-type doping, and in particular, p- doping levels was needed. As a result of this early work, a TMA bubbler was installed with the technical assistance of NASA-GRC[1].

2.1.4. 75 mm Cold-Wall CVD Reactor Implementation

In order to grow device-quality epi on 2" (50 mm) wafers a new CVD reactor was needed. Based on the success of the 35 mm reactor technology transferred from NASA-GRC, EMRL designed a scaled up version to accommodate wafers of up to 75 mm diameter (3") to permit the reactor to meet future substrate dimensions. The gas handling, control panel and reaction tube were completely redesigned to allow the conduct of repeatable, but flexible growth experiments.

An effective reaction tube design requires a laminar gas flow and optimal thermal conditions to ensure adequate thermal energy for film growth in addition to a flat temperature profile for epi growth uniformity. Fluid flow computations were made for a horizontal, atmospheric pressure cold-wall reactor to calculate the ideal flow geometry to satisfy these needs [3]. To accommodate a 75mm wafer, a flow width of 3½" was selected. From these calculations, the optimum projected flow area height and carrier gas flow were determined to be ½" and 6 slm, respectively. Computational fluid dynamics (CFD) simulations were performed at NASA Glenn Research Center, Lewis Field, and are shown below in Figure 2-3 [3].

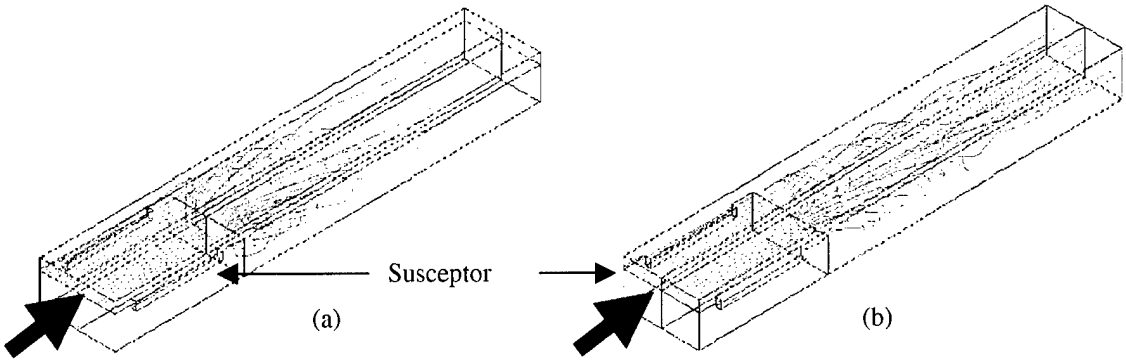


Figure 2-3. CFD analysis for 0.5" x 3.5" flow cross section for (a) 3 slm and (b) 6 slm carrier gas flow. Flow, as indicated by the arrows, is from lower left to upper right [3].

The first task was to reduce to practice the flow dimensions computed by Burke [3] and verified by CFD. Figure 2-4 shows both a photograph of the assembled tube and a photograph of the reactor during a 3C-SiC on Si growth run (2" (0001) Si substrate). This tube was fully assembled one year into the program and debugging of the hardware and software completed by the end of 1999.

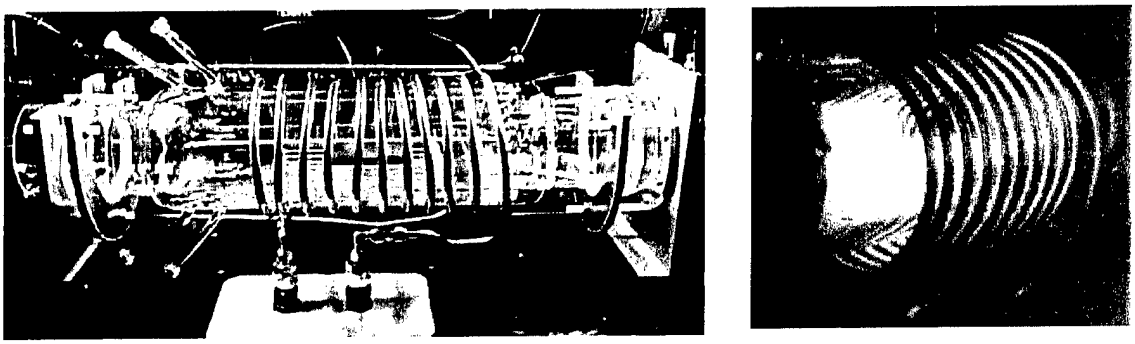


Figure 2-4. (a) Photograph of the assembled 75 mm tube. The stainless steel end plate is on the right and the RF induction coil is shown. (b) tube in operation.

A new control system was designed for the 75mm reactor to permit automatic startup and shutdown with an option to do either (or both) manually. While in manual mode, changes in procedure can be easily tested and implemented by the user. The final critical system to be upgraded for this program was the gas delivery system. Considerable care was taken to run welded (VCR fittings) stainless steel gas lines to all process gas manifold valves. A back-up hydrogen purifier was incorporated into the system to prevent down time due to purifier servicing. After vacuum and pressure testing the gas hardware, the upgraded 75 mm CVD reactor was ready for service.

First a scaled version of the 35 mm reactor graphite susceptor was fabricated and tested and the optimum geometry for uniform growth temperature obtained. The next step was susceptor manufacturer qualification. A systematic series of growth experiments were performed on various vendor susceptors and the epi analyzed to determine the background doping in the epi layers. Compensated doping levels obtained from C-V measurements and PL data taken in-house were compared for all suppliers. PL data indicated that films grown on susceptor A has an Al peak that is nonexistent in the film grown on susceptor B. Therefore epi growth on susceptor B will be of higher purity than susceptor A. Based on these experiments, susceptors from the best source (vendor B) were ordered and systematic growth experiments conducted with the goal of achieving whole-wafer, uniform epi.

Once the 75mm reaction tube design and construction was completed, systematic growth studies were conducted to validate the various designs and to establish operating points for CVD epitaxial layer growth.

2.1.5. Epitaxy Progress and Achievements

To find the operating points for the new reactor, several experiments were performed. First epi morphology was investigated and the optimum gas flow rates were determined. Next a tight series of growth experiments were performed starting with a Si/C ratio of 0.5 and decreasing it to a minimum of 0.15. Figure 2-5 (a) shows a photo of the reactor during growth with a silicon cloud observed during these experiments. The observation of a silicon cloud has been reported to be evidence of a near ideal growth process [4].

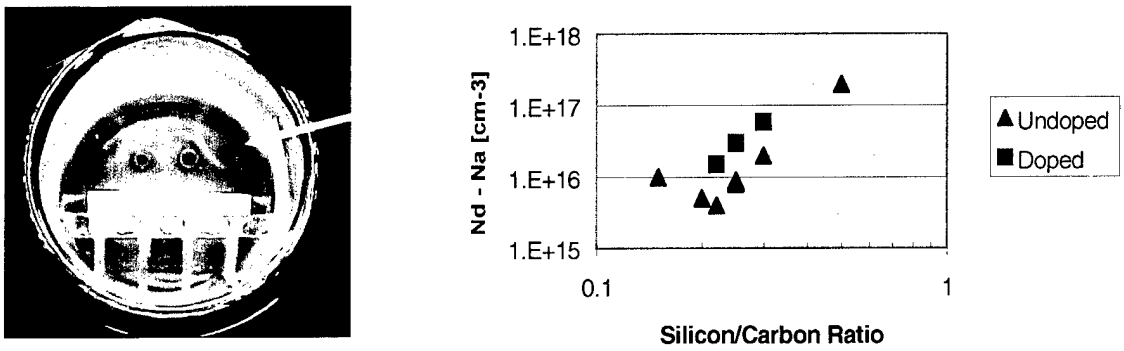


Figure 2-5. (a) Silicon saturation cloud (arrow indicate cloud position). (b) 75 mm reactor doping matrix for doped (pink squares) and undoped (blue triangles) epi runs.

The epi surface was pristine with excellent surface morphology. In this series of Si/C ratio experiments, the doping concentration varied from mid E15's to 2E17 cm^{-3}. At a Si/C ratio below 0.22, shallower donor/acceptor compensation was observed to begin. These results were repeated with different susceptors to verify process repeatability. Next growth experiments with these process set points were repeated with intentional nitrogen doping to increase the uniformity of the doping concentration throughout the layer thickness. Figure 2-5 (b) shows a growth matrix displaying the results of both intentional and unintentional doping experiments in the 75mm reaction tube, where the doping density is plotted as a function of the Si/C ratio.

Uniform epitaxial layer thickness is just as critical as uniform doping concentration for proper device operation. Cross-section SEM was used to monitor the growth rate and showed that the growth rate appears to be slightly higher than 2 μm/hr and uniform. Further research was conducted to increase the growth rate. By maintaining the same hydrogen flow rate and increasing the silane flow rate, the silicon to hydrogen ratio was increased which resulted in a growth rate of ~ 2.5 μm/hr. Next whole-wafer epitaxial layers were grown for a duration of 5 hours at the two growth rates discussed above (2.0 and 2.5 μm/hour). After 5 hours of epi growth, the first wafer had a 10.6 μm thick epi layer (as determined by SEM on a flag sample) while the second had a 12.6 μm thick epi layer. Both morphology and doping density control were maintained during these long growth experiments.

The last requirement was to verify doping uniformity across a full 35 mm wafer.

In both cases the surface was specular with no epi crown detected. This has been confirmed in a current ONR program with GECRD for both n- and p-type epi grown in this reactor. Vertical Ni Schottky diodes of 195μm diameter were then fabricated in-house on both wafers so that C-V measurements could be performed to map the 2-D doping density across the epi layers. The wafer was then probed on a micromanipulator probing station and C-V measurements were made with a HP 4280A capacitance meter. 2-D doping density maps are shown in figures 2-6 (a) and (b) for the 10.6 and 12.6 μm epi layers, respectively. These figures show a doping uniformity improvement with increasing precursor gas flow rates.

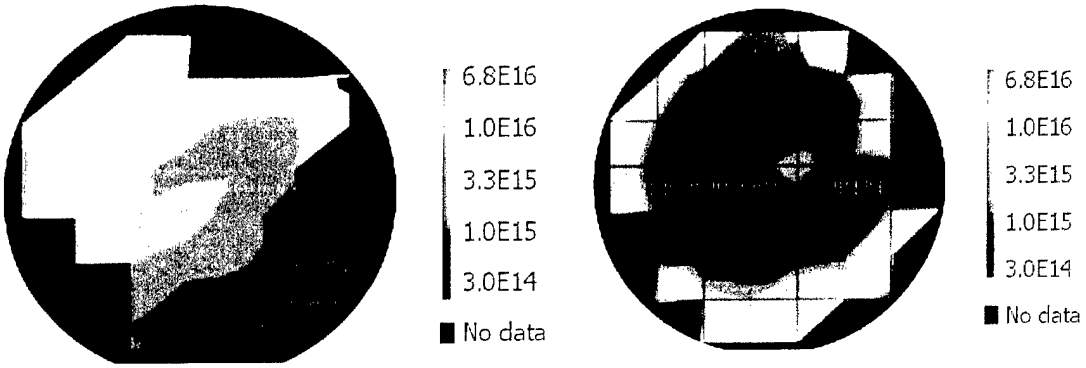


Figure 2-6. 2-D doping concentration map for the (a) 10.6 μm and (b) 12.6 μm thick whole-wafer epitaxial layers, respectively.

PL measurements were made in-house and SIMS performed at the Army Research Laboratory by Dr. Mark Wood on the flag samples from these two whole-wafer runs. The PL data indicate that with the exception of B, which is always present, the epi layer is very clean from other residual impurities. This result was confirmed by SIMS with Cr, Al and V all having concentrations below the SIMS detection limit.

2.1.6. Reduced Defect Density Epitaxial Layers

During this program growth studies were performed on reduced micropipe density substrates provided by TDI, Inc.[5]. The epi quality of these substrates was sufficient for Schottky diodes fabrication and testing. Preliminary data showed a three-fold increase in breakdown voltage for diodes made on this material compared with conventional substrates [6]. Due to space constraints the reader is referred to the literature for more information on this promising approach, which has the potential of producing epitaxial layers of sufficient quality for large-area device fabrication as needed for power switching applications.

2.1.7. Summary

During this work a new 75 mm CVD reactor was implemented. A full range of n-type epilayer doping density was achieved. After this program a full range of p-type doping density has also been achieved using a double-dilution TMA bubbler installed during the program. EMRL is now able to grow epi from 1E15 to >1E19 cm^{-3} of either n or p-type

on substrates of up to 3" (75 mm) due to the work accomplished during the SiC Megawatt Program.

One of the major problems faced by GE on epi material provided by Cree is a parasitic overgrowth referred to as 'epi crown.' Epi crown occurs when the layer is either thicker in the middle of the substrate or around the edges. Indeed, GE observed epi crown of up to 20-30 μm on material provided by Cree [7]. Being sensitive to this issue, we were careful to measure the epi flatness and found complete absence of epi crown on our epi layers of 10.6 and 12.6 μm. We consider this result as an important outcome of this research, because absolute epi flatness over the whole wafer is critical during device fabrication to achieve high resolution patterning without mask damage in contact lithography.

2.1.8. Future Work

Further enhancements of the reactor are planned. These include changing the operating point from atmospheric pressure to low pressure, increasing the precursor flow rate to increase the epi growth rate, and changing the design of the high-purity susceptor to permit growth on 3" diameter substrates which are beginning to enter the commercial market.

At the current growth rate of 2.5 μm/hour, it would take 20 hours to grow a 50 μm thick blocking layer. An increase to 5 μm/hour requires a growth run of only 10 hours. Operation at low pressure should increase the growth rate and permit a 5 μm/hour growth rate to be achieved in a cold-wall system [8]. In addition, it is well known that a warm-wall (and especially a hot-wall) reactor can achieve growth rates of up to 30 μm/hour [8]. The EMRL CVD reactor can be run in either mode with the proper installation of graphite parts and carbon foam insulation, thereby providing maximum flexibility for conducting advanced epi research.

2.1.9. Publications

T. E. Schattner, Homoepitaxial Growth of 4H and 6H-SiC in a 75mm Reactor, MS Thesis, Miss. State Univ., May 2000.

S. E. Saddow, T. E. Schattner, J. Brown, L. Grazulis, K. Mahalingham, G. Landis, R. Bertke and W. C. Mitchel, "Effects of Substrate Surface Preparation on Chemical Vapor Deposition Growth of 4H-SiC Epitaxial Layers," J. of Electronic Materials, accepted for publication, April 2001.

S. E. Saddow, T. E. Schattner, M. Shamsuzzoha, S. V. Rendakova, V. A. Dmitriev, "TEM Investigation of Silicon Carbide Wafers With Reduced Micropipe Density," Journal of Electronic Materials, 29 (3) (2000), 364-367.

S. E. Saddow, M. S. Mazzola, S. V. Rendakova, and V. A. Dmitriev, "Silicon Carbide CVD Homoepitaxy on Wafers With Reduced Micropipe Density," Mat. Science Engr. B, B61-62, (1999).

2.2. Trench Etching

SiC trench etching is needed to form the GTO mesa structure. In this process trench etching is used twice to form the recessed gate and the edge termination. The gate trench is shallow, typically 0.6 µm deep, to cut through the thin p+ anode layer and expose the n-base region to the gate contact. The edge termination trench is deeper, typically 2.0 µm, to penetrate through both the anode and n-base layers for exposing the p-base and allowing the formation of the junction termination extension (JTE). In both cases the trench must have nearly vertical walls with smooth bottom and sidewalls to achieve high cell density and high yield.

Despite many experimental studies and the investigation of various etching techniques reported in the literature, we found that SiC trench etching is still problematic if performed on a routine basis for device fabrication. We used Reactive Ion Etching (RIE) in an Anelva machine with a gas mixture of NF_3/O_2 at 4:1 ratio and 40 mTorr pressure. The power varied from 300 W to 400 W. A quartz cathode cover was used to avoid the possibility of backsputtering. Our standard etch mask was a stack of 2000 Å aluminum over 300 Å SiO_2. Several pre- and post-etch cleaning steps were used to ensure the removal of all particles that could affect etching uniformity or leave residues.

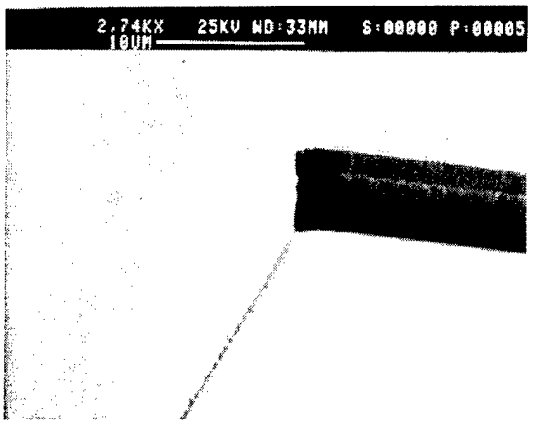


Figure 2-7. SiC trench with smooth bottom

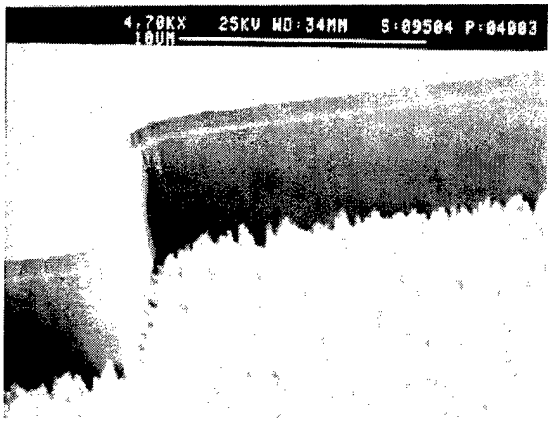


Figure 2-8. SiC trench with rough bottom surface caused by micromasking

Normally the above technique resulted in excellent trenches, as shown in Figure 2-7. However, a well-known trench etching problem, called micromasking, occurred from time to time, causing the formation of a "bed of nails" or "grass" at the bottom of the trench, as shown in Figure 2-8. These spikes consist of SiC residues, which originate from the masking action of aluminum particles redeposited on the trench surface during etching. Because of etching anisotropy, these spikes are not eroded sidewise during etching and continue to grow as the etching progresses, being more noticeable for deeper trenches.

This problem led us to try a different masking material using nickel instead of aluminum. The advantages of nickel are a reduced particle backsputtering rate and a higher etch rate with our etching conditions. The latter property should help to remove particles, which redeposit on the etching surface and cause micromasking. Moreover, our partner, Rensselaer Polytechnic Institute, had also switched to nickel for similar reasons. However, despite initial successes, the use of nickel did not show the desired trouble-free etching process, because of the sporadic appearance of micromasking and of a new trench defect, which is characterized by the formation of a comb-like residue near the sidewalls.

Figure 2-9 shows the above defect in two SEM micrographs at different magnification of a trench etched using a nickel mask. The comb-type residue is only evident at high magnification, because it is a small fraction, about $1/20^{th}$, of the trench depth. Its linear topology suggests that its origin is not due to masking particles, but to nickel/polymer stringers near the sidewalls. These stringers appear to be a parasitic phenomenon connected with the normal thin polymer coating of the trench sidewalls, which is an integral part of an anisotropic RIE process. This thin polymer is formed by nucleation on the sidewalls of free F and C radicals in the etch plasma. Therefore, while the vertical

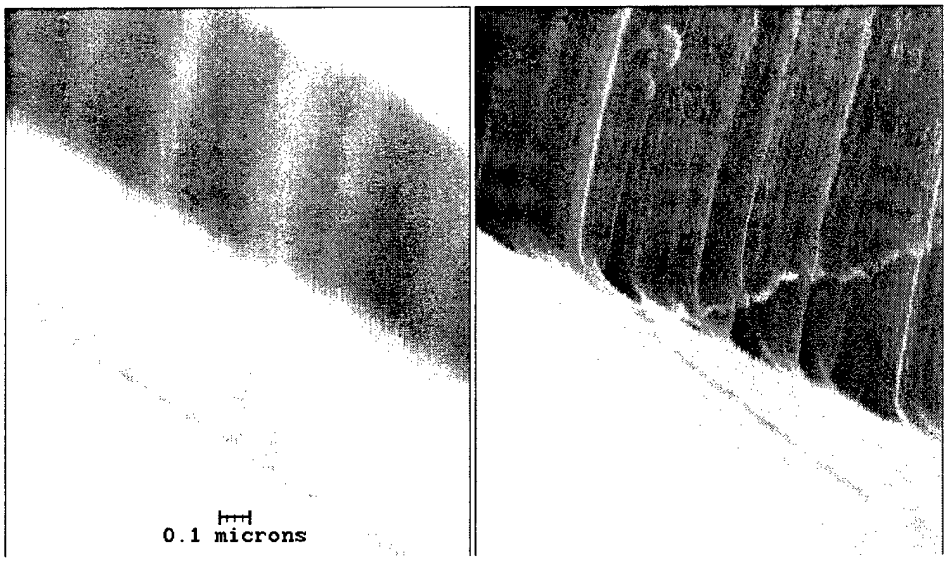


Figure 2-9. Comb-like residue on RIE etched trench bottom

surfaces are protected, the bottom is continuously eroded, because energetic ions bombardment prevents polymer formation on the bottom and hence exposes it to the chemical reaction with the plasma.

A possible cause of the stringers could be the lateral erosion of the nickel mask, because it could shift the masking edge during etching and therefore form a second etch front in the middle of the process. Consequently, the original polymer protected surface may be left behind forming a stringer lying parallel near the sidewall. This hypothesis is consistent with the fact that stringers were never observed with aluminum masking, whose lateral erosion rate is negligible during this RIE process.

Since many variables affect the etching quality and repeatability, we conducted a systematic experiment to adjust the RIE process and eliminate the occurrence of micromasking and stringers. The variables selected were:

1. Reduced RF power
2. Increased NF_3/O_2 flow
3. Inclusion of O_2 descum before and after etching
4. Addition of asher-clean to the post-etch clean

The experimental results did not identify a significantly improved operating point. The main conclusion was that a trade-off exists between achieving a high level of anisotropy with the associated risks of micromasking and stringers, and accepting a more isotropic etch profile. Nevertheless it is possible that these limitations will be removed with the use of advanced RIE equipment with computer control of the etch cycle, which will allow pulsing between isotropic and anisotropic etching conditions. Consequently residues will be removed as they are formed, leaving a smooth trench surface without compromising on the aspect ratio or the profile anisotropy.

2.3. Ion Implantation

2.3.1. Ion Implantation for High Voltage SiC Power Devices

Ion implantation is the only mean available for planar selective area doping of SiC. This is because the diffusion constants of the most important dopants are extremely small at reasonable temperatures, which do not cause surface degradation. In SiC high power device technology selective area ion implantation doping is required to form various regions of desired sheet resistance and depth in diodes, transistors, MOSFETs, IGBTs and thyristors. Key advantages are accurate doping concentration and range, conservation of surface planarity even in stacked n- and p-type regions, MOSFET threshold adjustment and contact resistance reduction by means of local implants. Ion implantation also offers the potential of source/drain self-alignment in MOSFETs, although this capability depends on developing a lower temperature implant anneal to avoid gate damage. Moreover, non-dopant ion implantation is useful in high power SiC devices for edge termination of high blocking voltage.

In this work, we have developed empirical formulas that can accurately predict the range statistics of various acceptor and donor dopants in the energy range from 50 keV to 4 MeV, based on experimental results. We have also determined the optimum annealing conditions that result in reproducible electrical characteristics without deteriorating the surface morphology for both donor (N, P, As, and Sb) and acceptor (Al, B, and Ga) impurities. The dependence of sheet carrier concentration and residual lattice damage as a function of ion implantation dose was also studied for some of the important dopants. Using optimum implantation/annealing conditions, planar n-p junction diodes were fabricated utilizing double-implantation technology.

2.3.2. Range statistics

To develop the empirical range statistics formulas for N, P, B, Al, and Ga ions, single energy ion implantations were performed at various energies in the range 50 keV to 4 MeV, at a peak dopant concentration of $\approx 1x10^{20}$ cm^{-3}. Secondary ion mass spectrometery (SIMS) depth profiles of the individual implants were analyzed using the following formulas to extract the range statistics at various ion energies [9]:

$$\text{Normalized concentration } f(x) = \frac{N(x)}{\int_{-\infty}^{\infty} N(x)dx} \quad \text{(i)}$$

$$\text{Average Range } (R_p) = \int_{-\infty}^{\infty} x f(x)dx \quad \text{(ii)}$$

$$\text{Straggle } (\Delta R_p) = \left[\int_{-\infty}^{\infty} (x - R_p)^2 f(x)dx\right]^{\frac{1}{2}} \quad \text{(iii)}$$

$$\text{Skewness } (\gamma) = \frac{\int_{-\infty}^{\infty} (x - R_p)^3 f(x)dx}{R_p^{\,3}} \quad \text{(iv)}$$

$$\text{Kurtosis } (\beta) = \frac{\int_{-\infty}^{\infty} (x - R_p)^4 f(x)dx}{R_p^{\,4}} \quad \text{(v)}$$

By obtaining the range statistics derived from the SIMS profiles using the above formulas, empirical formulas were then developed by fitting these points over the energy range used [9]. The empirical formulas and the constants for acceptor dopants are given below:

$$\text{Range of maximum concentration } (R_m) = k_1 (E - k_2)^r \quad (1)$$

$$\text{Mean range } (R_p) = k_3 (E - k_4)^s \quad (2)$$

$$\text{Straggle } (\Delta R_p) = k_5 (E - k_6)^t \quad (3)$$

$$\text{Skewness } (\gamma) = k_7 \left[(E - k_8)^u - 1.2\right] \quad (4)$$

$$\text{Kurtosis } (\beta) = \frac{\left[39\gamma^2 + 48 + 6(\gamma^2 + 4)^{3/2}\right]}{32 - \gamma^2} + k_9 E + k_{10} \quad (5)$$

$$\text{Max. Concentration / Dose } (N_m / \phi) = k_{11} \left[(E - k_{12})^v + 1\right] \quad (6)$$

In the above formulas, E is the ion implant energy in MeV. The fitting parameters for acceptors to introduce into equations (1) through (6) are given in Table 2-1.

Table 2-1. Fitting parameters for acceptor empirical formulas

	k_1 (μm)	k_2 (MeV)	k_3 (μm)	k_4 (MeV)	k_5 (μm)	k_6 (MeV)
B	1.2	-0.030	1.2	-0.017	0.093	0.046
Al	0.93	0.045	0.91	0.042	0.14	0.048
Ga	0.55	0.044	0.53	0.029	0.12	0.020

	k_7	k_8 (MeV)	k_9 (MeV^{-1})	k_{10}	k_{11} (cm^{-1})	k_{12} (MeV)
B	6.8	0.047	0.30	0.96	$2.9x10^4$	0.037
Al	3.5	0.045	0.24	0.81	$1.7x10^4$	0.024
Ga	-1.3	-0.033	0.037	-0.0019	$1.7x10^4$	-0.017

	r	s	t	u	v
B	0.76	0.75	0.16	-0.029	-0.24
Al	0.64	0.64	0.26	-0.072	-0.57
Ga	0.87	0.85	0.60	0.39	-1.0

The empirical formulas and fitting constants for the donor dopants can be found in reference [10]. Knowledge of these empirical formulas is very helpful to model the implant depth profiles for a given ion energy and dose by substituting these moments into the Pearson IV distribution function. We observed that the Pearson IV distribution together with these empirical formulas can predict the implant distributions more closely than computer codes such as TRIM, especially in the MeV energy range. Pearson IV fitting to the SIMS data based on the empirical formulas and TRIM modeling depth profiles for 3 MeV Al, B, and Ga implants are shown in Figure 2-10. We observed that the range statistics for a given dopant were similar in both the 6H and 4H polytypes of SiC.

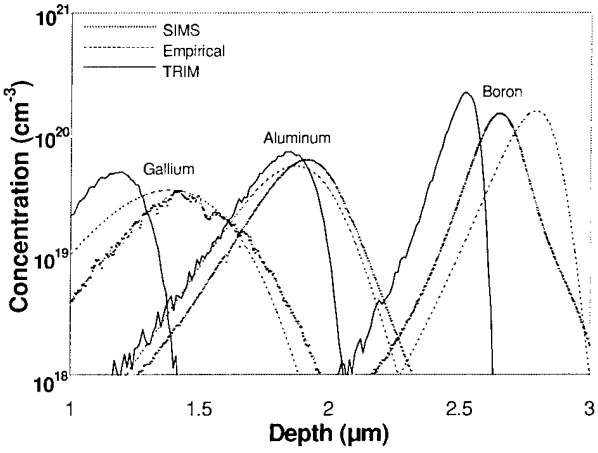


Figure 2-10. Implant depth profiles generated by experimental SIMS, TRIM modeling, and Pearson IV modeling from empirical formulae for 3 MeV Al, B, and Ga implantations.

2.3.3. Surface Morphology

In this work, to study the effects of heat treatments on the surface morphology, annealings were performed on implanted and unimplanted SiC material in the temperature range 1300 °C to 1600 °C. At first the anneals were done without any deposited capping layer, encasing the samples in an amorphous SiC crucible with a piece of single crystal SiC placed on the sample surface. It was observed, using atomic force microscopy (AFM), that the surface deteriorated at high (> 1300 °C) annealing temperatures, with long furrows running across the surface with their depth increasing with increasing annealing temperature and time. This phenomenon is popularly called

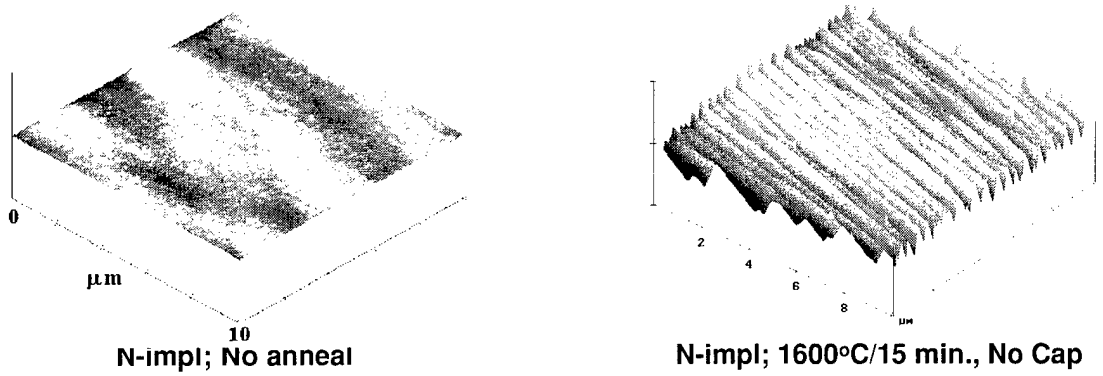


Figure 2-11. Atomic force micrographs of the SiC surface of the as-implanted and annealed samples for different encapsulant conditions.

'step bunching'. The furrows were created by adsorption of Si-containing species, such as Si, SiC_2, Si_2C, etc., caused by sublimation during high temperature annealing. For 1600 °C / 15 minutes annealing these furrows were as deep as 20 nm in the implanted material [11]. The depth of the furrows also depended on the degree of implantation damage. For example, the furrows are deeper in the implanted material as compared to the unimplanted material cut from the same wafer. Also, the depth of the furrows increases for heavier ion implant species as compared to lighter species for the same implant dose. Formation of these furrows must be eliminated for fabricating reliable high power SiC devices using ion implantation.

To avoid the sublimation related surface damage, we have annealed SiC implanted with various dopants using an AlN cap [12]. The AlN cap was pulse-laser-deposited on the SiC surface after ion implantation and before annealing. The annealings were performed in an RF furnace using a graphite susceptor in argon ambient. SiC proximity is also used on the sample surface during this annealing. The AFM results showed that the AlN encapsulant prevents the formation of long furrows on the SiC surface for annealing at temperatures as high as 1600 °C for 15 minutes. However, deterioration of the AlN cap was observed at temperatures of 1650 °C if the annealing time is more than 15 minutes, or even at 1600 °C for very long (>30 minutes) anneals. AFM micrographs with different annealing conditions are shown in Figure 2-11 for N-implantation. The AlN cap is also found to be effective in preventing the out-diffusion of dopants such as As, Sb and Ga. However, for the case of B, out-diffusion of the dopant still occurred near the surface region [9].

2.3.4. Donor Implantation Results

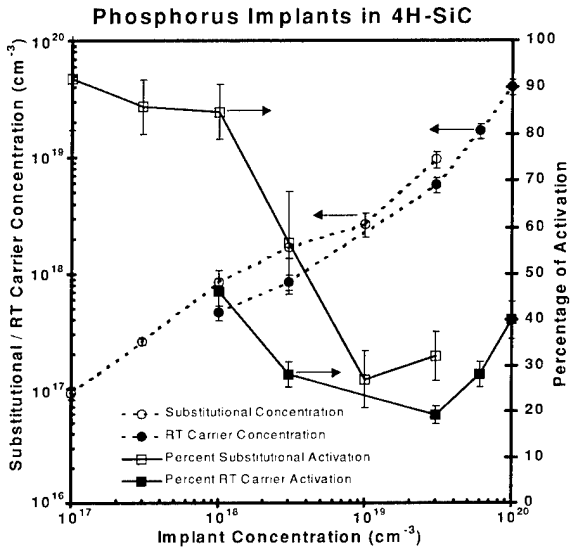


Figure 2-12. Variations of room-temperature carrier concentration, substitutional implant concentration, and the corresponding percentages of activation versus the P-implant concentration in 4H-SiC. The implants were performed at 700 ºC and annealed at 1600 °C, except for 6 x 10^{19} cm^{-3}, which was annealed at 1650 °C.

It is well known that nitrogen is an attractive donor species in SiC because of its lighter mass. In this work, for multiple energy nitrogen implantations performed at 500 °C in 4H-SiC we measured a room temperature sheet resistivity of ≈ 70 Ω / □ for a 1.0 μm deep, $2x10^{19}$ cm^{-3} box profile N-implant, annealed at 1500°C for 15 minutes [11]. However, the sheet resistivity increased for higher nitrogen implant concentrations because of the formation of electrically inactive nitrogen complexes at these concentrations. It seems that the nitrogen implantation is useful to achieve donor concentrations only up to ≈ $2x10^{19}$ cm^{-3} with no additional benefit of using higher concentrations. We also obtained almost similar nitrogen implant activation whether the implants were performed at room temperature or at an elevated temperature when the nitrogen concentration is ≤ $2x10^{19}$ cm^{-3}. At these doping concentrations, a typical substitutional N activation is 80 - 100% with corresponding room temperature carrier concentration of roughly 30%. This is due to the ≈ 80 meV donor activation energy of nitrogen in SiC.

Figure 2-12 shows the percentage room temperature (RT) carrier activation dependence on implant concentration for phosphorus implants performed at 700 °C with a 0.45 μm deep box profile. The percentage RT carrier activation is defined as the ratio of RT sheet carrier concentration to implant dose. Initially the percentage RT carrier activation decreased with increasing dose (from 46% for $1x10^{18}$ cm^{-3} to 17% for $3x10^{19}$ cm^{-3}) due to increased lattice damage for implant concentrations up to $3x10^{19}$ cm^{-3} [13]. Unlike nitrogen, at higher (> $3x10^{19}$ cm^{-3}) phosphorus implant doses, the carrier activation increased with increasing implant dose. This is most likely because of the absence of electrically inactive P complexes that enables the merging of the P donor band with the conduction band resulting in higher possible carrier activation for phosphorus. For a multiple energy $1x10^{20}$ cm^{-3} P implant, a carrier concentration of $4x10^{19}$ cm^{-3} was measured at room temperature with a corresponding sheet resistivity of 110 Ω / □ and a carrier mobility of 30 cm^2 / V·s. The room temperature phosphorus implantations yield very poor carrier activations at high doses due to very high lattice damage, and are not useful for high power device applications.

Based on the above nitrogen and phosphorus implantation results, the elevated temperature high-dose phosphorus implantation is preferred over nitrogen implantation to obtain low resistance contacts required for SiC high power devices. Despite using elevated temperature implantation, a relatively high degree of residual lattice damage remains for P-implantation compared to N-implantation for high (> $1x10^{19}$ cm^{-3}) implant doses. This could pose a problem by increasing p-n junction leakage currents. The nitrogen implants are useful for obtaining deep lightly doped regions of multi-layer high power devices, and are also attractive because they can be performed at room temperature, which does not require any complicated high-temperature implant masking techniques.

In our study of elevated temperature (800 °C) As and Sb implants in 6H-SiC we obtained about 30% and 10% carrier activation at room temperature for approximately $1x10^{19}$ cm^{-3} As and Sb concentrations, respectively, when the annealings were performed at 1600 °C for 15 minutes using an AlN cap [12]. These values seem to be useful for device applications if one desires shallow, abrupt junction profiles. However, for room temperature As and Sb implantations, the activations were very low due to a high degree of residual implantation damage which also resulted in larger p-n junction leakage currents [14].

2.3.5. Acceptor Implantation Results

All acceptor implants in this study were performed at an elevated temperature (700 °C - 800 °C). For a box profile 10^{20} cm^{-3} Al implantation we obtained electrical activations (ratio of hole concentrations measured at room temperature to the total implant dose) of ~0.3% and ~1% after 1500 °C / 15 min. and 1600°C / 15 min. annealing, respectively [9]. The sheet resistance obtained for 1600 °C annealing is $1.2x10^4$ Ω / □ for a 1.0 μm depth 10^{20} cm^{-3} box profile Al implant. For boron, no room temperature carrier activation was

observed for annealing temperatures less than 1650 °C. After 1650 °C annealing we observed 0.01% activation, which increased to about 0.1% after 1700 °C annealing. For box profile 10^{20} cm^{-3} gallium implants the room temperature carrier activation was measured at about 1% after 1700°C annealing. The low hole concentrations measured at room temperatures are due to the high carrier ionization energies, ($E_A \approx$ 240-350 meV) of these acceptors in SiC.

The C-V profiling on lightly doped material yielded substitutional Al concentrations of $7x10^{16}$, $2x10^{17}$, and $5x10^{17}$ cm^{-3}, respectively for $1x10^{17}$, $3x10^{17}$, and $1x10^{18}$ cm^{-3} Al implants. These values represent a substitutional Al activation of 50-70% for 1600 °C annealing. For $1x10^{18}$ cm^{-3} B implants annealed at 1650 °C for 10 min., C-V profiling resulted in a substitutional B concentration of $8x10^{17}$ cm^{-3}, which corresponds to a substitutional activation of 80%. These results indicate that low doping concentration acceptor implants can be successfully used for multi-layer high power device applications. Using Al or B followed by N-implantations we made planar diode structures with good switching characteristics.

2.3.6. Doubly Implanted Planar n-p Junction Diodes

Doubly implanted, planar, circular (245 μm diameter) n-p junction diodes were fabricated in n-type ($4x10^{15}$ cm^{-3}) 4H-SiC epilayers grown on n+ 4H-SiC substrates using a sequence of p- and n- implants. A deep (1.0 μm) box profile was formed by multiple energy Al or B implants, followed by a shallow (0.2 μm) N-implanted box profile [15]. All implants were performed at 700 °C using either a thick (2.5 μm) SiO_2 layer or a Ni-plated layer with a Si_3N_4 buffer as the high temperature implantation mask. The diodes were annealed at 1650 °C for 10 minutes using an AlN encapsulant. Diode passivation was achieved using a 0.4 μm thick SiO_2 layer. No junction termination was used.

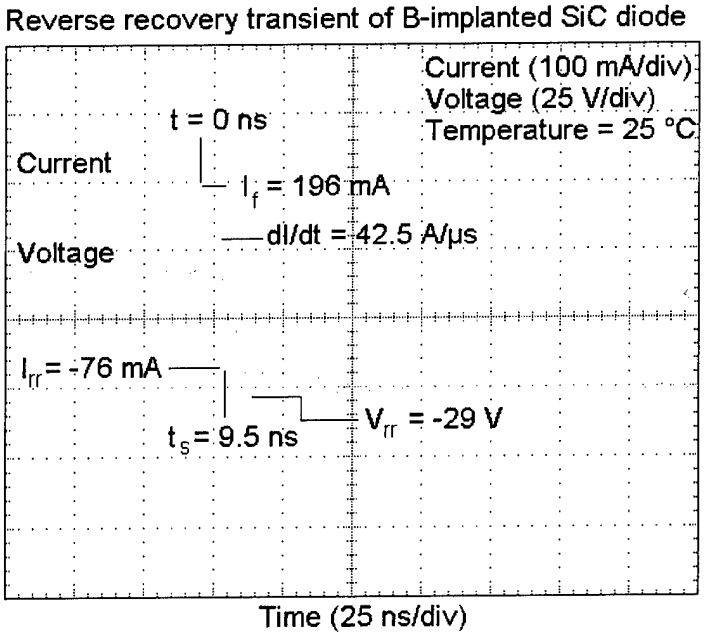


Figure 2-13. Reverse recovery transient of B and N implanted SiC diode

Diodes that were made by this double implantation technology

exhibited attractive I-V and switching characteristics. At room temperature, the B-implanted diodes exhibited a reverse leakage current of $5x10^{-8}$ A/cm^2 at a reverse bias of -20 V and a carrier lifetime of 7.4 ns. Reverse recovery characteristics of the B/N-implanted diodes are shown in Figure 2-13. No implantation-induced damage was observed using the EBIC imaging technique. The carrier lifetime calculated from the switching characteristics in doubly implanted diodes is similar to the value reported in devices made by n+ implantation in p-type epilayers. This indicates that the crystal quality of the thick p-type layer created by high-energy implantation is comparable to the p-type epitaxial layer. It is anticipated that the technology pursued in this work can be used for the development of more complex high power silicon carbide switching devices that require double- or triple-implantations.

2.3.7. Publications

E.M. Handy, M.V. Rao, O.W. Holland, P.H. Chi, K.A. Jones, M.A. Derenge, R.D. Vispute, and T. Venkatesan, "Al, B, and Ga ion implantation doping of SiC", J. Electron. Mater., Vol. 29, No. 11, 2000.

M.V. Rao, J. Tucker, O.W. Holland, N. Papanicolaou, .P.H. Chi, J.W. Kretchmer, and M.Ghezzo, "Donor ion-implantation doping into SiC", J. Electron. Mater. Vol. 28, p. 334, 1999.

M.V. Rao, J.B. Tucker, M.C. Ridgway, O.W. Holland, N. Papanicolaou, and J. Mittereder, "Ion-implantation in bulk semi-insulating 4H-SiC", J. Appl. Phys., Vol. 86, No. 2, pp. 752-757, 1999.

E.M. Handy, M.V. Rao, K.A. Jones, M.A. Derenge, P.H. Chi, R.D. Vispute, T. Venkatesan, N.A. Papanicolaou and J. Mittereder, "Effectiveness of AlN encapsulant in annealing ion-implanted SiC", J. Appl. Phys., Vol. 86, No. 2, pp. 746-51, 1999.

E.M. Handy, M.V. Rao, O.W. Holland, K.A. Jones, M.A. Derenge, N. Papanicolaou, "Variable-dose (1017-1020 cm -3) phosphorus ion implantation into 4H-SiC." J. of Appl. Phys., Vol.88, No.10, pp.5630-4, 2000.

J.B. Tucker, M.V. Rao, O.W. Holland, P.H. Chi, G.C.B. Braga, J.A. Freitas, Jr., N. Papanicolaou, "Material and n-p junction characteristics of As- and Sb-implanted SiC", Diam. Rel. Mater., Vol. 9, pp. 1887-96, 2000.

J.B. Tucker, M.V. Rao, N. Papanicolaou, J. Mittereder, A. Elasser, B. Clock, M. Ghezzo, O.W. Holland, and K.A. Jones, "Characteristics of planar n-p junction diodes made by double-implantations into 4H-SiC", IEEE Trans. Electron. Dev., in review.

2.4. MOS Gate Dielectric

Proper functioning of any metal-oxide-semiconductor field-effect transistor (MOSFET) depends critically on the semiconductor-oxide interface characteristics. Desired MOS characteristics include a low effective fixed charge density (Q_f) and a low density of interface states (D_{it}).

The situation for SiC MOSFET technology is no exception. Typical values for the fixed charge density in 4H-SiC fall into the range of 1-5 x 10^{12} cm^{-2}, and values for the density of interface states have been reported to be as low as the mid-10^{10} cm^{-2} eV^{-1} near the middle of the 4H-SiC band gap [16]. Unfortunately, the density of interface states increases exponentially near the conduction band edge, with D_{it} exceeding 10^{13} cm^{-2} eV^{-1} in some cases [16].

High D_{it} values are suspected as being a principal reason why the channel mobility is so poor in 4H-SiC MOSFETs. Previous measurements have shown the channel mobility to increase as the annealing temperature for source/drain implants decreases [17]. In those measurements, the gate oxide was thermally grown. More recent measurements have shown that channel mobilities can be as high as 70 cm^2/Vs if a deposited oxide is used in processing 4H-SiC MOSFETs [18]. However, a quantitative relationship between channel mobility and MOS interface characteristics has not yet been established.

As indicated by this brief overview, there are many unanswered questions about optimal processing of SiC MOSFETs. For this reason a joint experiment was designed between GE CRD and Purdue University. The objectives were:

- Evaluate various methods of gate oxide formation, i.e. thermal growth, CVD deposition, or a combination of these techniques.
- Evaluate the oxide quality dependence on the SiC surface, i.e. epi layers, 6H and 4H polytypes, implanted regions annealed at various temperatures.
- Characterize the oxide quality using C-V curves and measure the flatband voltage.
- Determine a preferred gate oxide formation method for the SiC DIMOS FETs being developed under this program.

A first group of oxides were deposited at GE CRD and sent to Purdue for evaluation. These were processed into capacitors and characterized by C-V measurements. One of these was a deposited oxide without the 950 °C reox treatment, and the other with the reox. Both were on p-type 4H-SiC doped to ~3 x 10^{15} cm^{-3}. The results were:

p-type, HTO oxide, without reox	V_{FB} = -22 V
p-type, HTO oxide, with reox	V_{FB} = -8 V

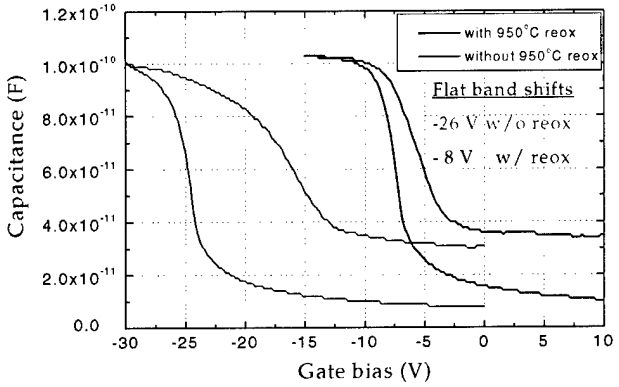


Figure 2-14. C-V curves of MOS capacitors with deposited oxides

These results show, as expected, that the reox anneal reduces the slow trap density and interface state density, D_{it}, as demonstrated by the decrease of flat band voltage shift, V_{FB}. Therefore, the inclusion of the reox anneal in the DIMOS process appears to be necessary. Figure 2-14 shows the C-V curves for the deposited oxides, where one can see the flat band voltage difference associated with the presence or absence of the reox treatment.

To further reduce V_{FB} a second set of deposited oxide samples was attempted. This followed attempts to deposit epitaxially AlN as a gate insulator for SiC MOSFETs. Although the formation of AlN was confirmed by x-ray diffraction, the MOS capacitors were very leaky and in the interest of time further experiments with this approach were deferred to a longer-term program.

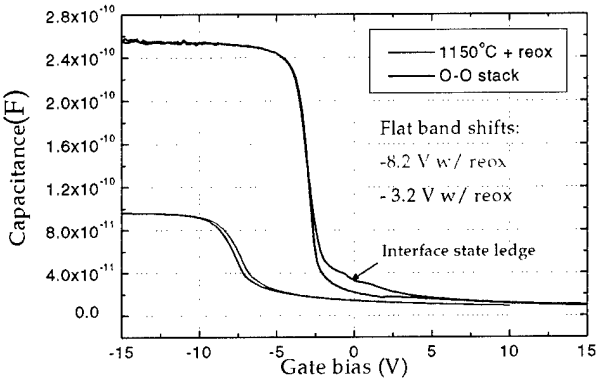


Figure 2-15. C-V curves of MOS capacitors with a single steam oxide layer and with a thermal/deposited double oxide stack

The second deposited oxide run included four samples: two n-type and two p-type, all on 4H material. The main goal was to investigate the effect of adding a reox anneal to steam oxidization, since its beneficial effect on interface states reduction has been widely reported. Another objective was a comparison of MOS properties between thermal growth of the entire oxide in steam and a combination of thermal oxidation and high temperature oxide (HTO) deposition. The second technique allows reducing the oxidation temperature, because the thermal oxide can be thinner, since the HTO layer provides the thickness balance.

The C-V results for these oxidation conditions were:

n-type, 1100 °C steam oxide	$V_{FB} = 2.2$ V
p-type, 1100 °C steam oxide	$V_{FB} = -9.8$ V

n-type, 1050 °C steam, 900 °C HTO, 950 °C reox V_{FB} = 2.6 V
p-type, 1050 °C steam, 900 °C HTO, 950 °C reox V_{FB} = -3.6 V

For n-type substrates, which are used for p-channel MOSFETs, steam oxidation alone appears adequate to provide a low V_{FB} value. Instead for p-type substrates, used for n-channel MOSFETs, the oxide stack with reox appears definitely superior, because it yields a V_{FB} value less than half of that of steam oxide. This result is graphically displayed in Figure 2-15, which shows the C-V curves for two MOS capacitors on p-type wafers, one with a 1150 °C steam oxide + reox and the other with an oxide-oxide (O-O) stack including reox.

A third set of samples was run to determine the effect of adding a 950 °C reox to the 1100 °C steam oxide for comparison with the previous experiments. The results were:

n-type, 1100 °C steam oxide, 950 °C steam reox V_{FB} = 5.0 V
p-type, 1100 °C steam oxide, 950 °C steam reox V_{FB} = -7.8 V

These results are inferior to those of the thermal oxide/HTO stack with reox, because of their higher V_{FB} values. Therefore, the double oxide stack with HTO and reox appears to be the preferred gate oxide formation technique among those investigated here.

Conductance measurements on MOS samples made on n-type wafers with this combination of thermal and deposited oxide showed D_{it} values near the conduction band edge of less than 1e12 $cm^{-2}eV^{-1}$. This is an excellent result that generated great excitement about the merit of the new gate oxide formation method. Unfortunately, it was later discovered that some samples were fabricated on 6H-SiC wafers instead of 4H leading us to defer to further experimentation a definitive conclusion on the D_{it} values for 4H material.

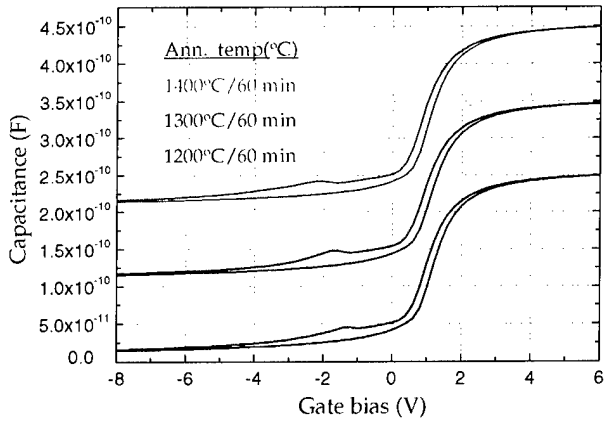


Figure 2-16. C-V curves of MOS capacitors formed on annealed n-type SiC wafers at temperatures between 1200 °C and 1400 °C

The n-channel DIMOS process requires p-type wafers. From Figures 2-14 and 2-15 it is easy to see from the flatband voltage that (1) the reox anneal improves the oxide quality and, (2) the stacked oxide is very good in terms of small flatband voltage shift, low interface states density and slow oxide traps. The comparison with steam oxide alone is validated by the use of the same epi wafer for both conditions. The D_{it} value for the oxide stack is much lower than for the steam oxide and corresponds to a shorter interface state ledge.

In the Megawatt program the DIMOS structure requires that an N-channel MOSFET be fabricated over an implanted p-base. This requires a high temperature treatment for implant activation of the p-base before gate oxide formation. Figure 2-16 shows the effect of this treatment on the C-V curves as a function of annealing temperature in the range of 1200 °C to 1400 °C. For this experiment thermal oxides were used with n-type wafers without performing the p-base implant. The figure shows that the higher the annealing temperature the wider is the interface states ledge with consequent increase of D_{it} and consequent decrease of effective channel mobility.

The combination of these results with current knowledge of SiC MOS technology led to the following recipe for the DIMOS gate oxide. First, any residual carbon from the ion implantation and activation anneal should be removed from the surface with an O_2 plasma clean or light RIE. This is necessary to avoid leakage through the oxide. A plasma clean is needed, because N_2 anneals are usually not done to remove carbon during sacrificial oxidation, and the RCA clean does not remove it. After plasma clean, a thorough RCA clean is needed. The thermal/deposited oxide stack is the preferred gate oxide formation technique. A suitable recipe is as follows:

Load under dry O_2 condition at ~650 °C into the thermal oxidation tube
Ramp to 1050 °C over 10-20 min in dry O_2
Switch to steam at 1050 °C and oxidize for 1 hour
Switch back to dry O_2 and continue for ~10 min (to drive off H_2O and CO vapors)
Ramp down to 650 °C to remove the wafers from the thermal oxidation tube
Load into the HTO tube
Deposit HTO at 900 °C using the standard procedure (do not thermally shock wafers)
Perform standard reox anneal at 950 °C in steam

Although these oxidation conditions should improve the MOS properties, the formation of NMOS FETs over an implanted surface is still problematic in SiC. Particularly in 4H SiC the channel mobility can be as low as 1 cm^2/Vs. To a large extent the mobility is a function of the surface conditions after the high temperature anneal for p-base implant activation. The use of silane overpressure should help to avoid "step bunching" and lead to higher mobility. Another approach will be the use of a buried channel to improve the carrier transport properties by separating the channel from the interface traps and scattering centers.

2.5. Implant Annealing

2.5.1. Conventional Implant Annealing in SiC

Ion implant activation, normally referred to as Implant Annealing (IA), is a difficult process to perform in SiC due to the strong covalent Si-C bonds. In order to electrically activate ion implants, the interstitial atoms must become substitutional in the crystal lattice. Therefore Si-C bonds must be broken so that interstitial dopant atoms can replace either a C atom (N doping) or Si atom (B or Al doping). Clearly, once the Si-C bonds are broken at the SiC surface, damage to the surface can occur due to out-diffusion of lattice

atoms. This is a well-known problem in SiC IA, which results in a rough surface morphology referred to as "step bunching". This roughness originates from SiC surface etching at high temperature caused by Si out diffusion, as proven by a residual high C content on the surface after IA. These conditions occur for all the conventional processes, mainly vacuum, capped and Ar high-temperature anneals [19].

2.5.2. Capped Annealing

One method commonly used to prevent surface damage is to employ an annealing cap. There are various methods ranging from the use of another SiC wafer to form a sandwich to the deposition of refractory materials over the SiC wafers to suppress surface atom mobility and out diffusion. Jones et al have successfully used a deposited AlN cap up to an IA temperature of 1500 °C [20]. Unfortunately this temperature is not adequate for B or Al activation since these species require IA temperatures in excess of 1600 °C. Spencer et al employed a graphite cap in a process whereby photoresist was converted to C in a CVD system [21]. This process has proven successful but difficult to work with since it involves the oxidation and stripping of the graphite layer after the anneal with the possibility of leaving a graphite surface residue. Perhaps the most successful IA process developed thus far is by Williams et al at Auburn University [22]. This process requires a specially designed and machined graphite pill box. If properly configured there are no temperature gradients across the sample during the anneal and the original surface morphology is maintained. While the current physical size is limited to small (~1 cm) samples, scaling to larger size should be possible provided that adequate temperature uniformity is maintained.

2.5.3. Vapor Overpressure Annealing

Rottner et al in Sweden successfully demonstrated a process whereby silane was used to provide an overpressure of Si during the IA process [23]. This process is similar to arsenic overpressure IA that is commonly employed in the GaAs material system. This approach, which is literally a 'virtual cap', was shown to prevent step-bunching in high-temperature annealing of SiC implanted material. However, insufficient information was provided and therefore process transfer to the USA hampered. The Emerging Materials Research Laboratory (EMRL) at Mississippi State University set out to develop a silane overpressure IA process to duplicate the results of the Swedish group [24].

2.5.4. Development of Silane Overpressure Annealing Process

A silane-based CVD reactor suitable for performing high-temperature anneals in a silicon rich ambient was used for these experiments. Annealing temperatures in excess of 1700 °C are possible by placing the sample to be annealed on a SiC-coated graphite susceptor and heating the graphite using an RF induction coil. The thermal process schedule developed during this research is shown in Figure 2-17, while processing details have been reported in the literature [25]. RBS and AFM data taken after a 1600 °C IA on Al implanted n-type epi layers are shown in Figure 2-18. A comparison with pre-IA AFM

micrographs (not shown) indicates that the no crystallographic damage occurred to the surface during the IA process.

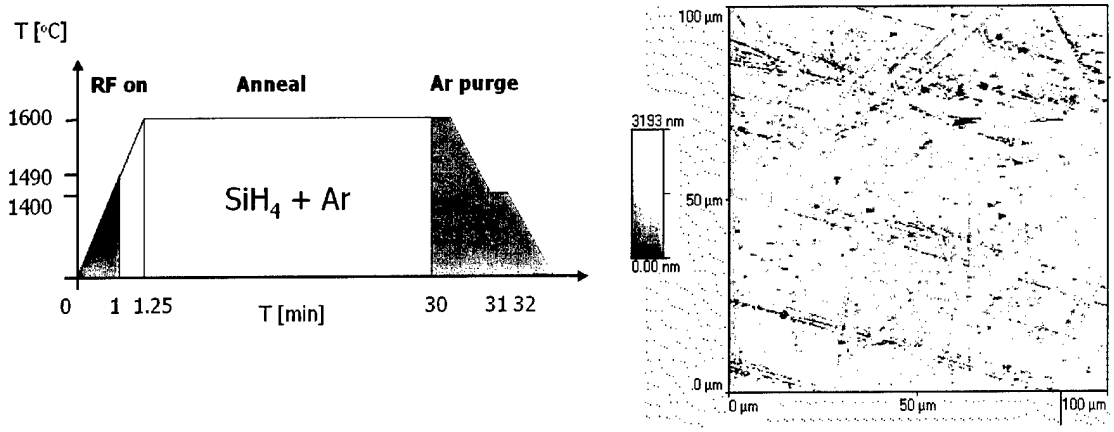


Figure 2-17. (a) 1600 °C IA process thermal schedule indicating gas flow timing. (b) AFM image of surface after IA at 1600 °C. Surface is improved over pre-IA morphology (not shown).

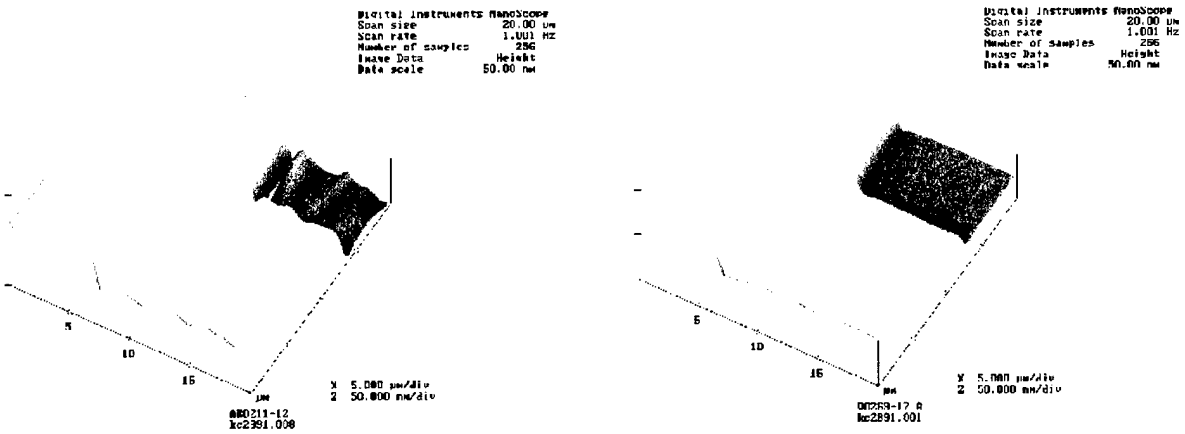


Figure 2-18. AFM images of surface quality (a) after 1500 °C Ar anneal; (b) after 1600 °C IA using the silane overpressure process. Ar annealed surface is rougher even at lower temperature.

Once the basic IA process was demonstrated, annealing experiments were performed at temperatures of 1400, 1500, 1600, and 1700 °C, respectively. In an effort to prevent elemental Si from forming on the crystal surface during the 1400 °C anneal, the flow was cut back to 60 sccm. In addition to inspection of the crystal surface using optical microscopy, the surface chemistry was evaluated using XPS. An XPS survey conducted on the heaviest doped (1E19 cm-3) sample annealed at 1700°C indicated that with the exception of O, which is in the form of SiO2 at the surface of this air-exposed sample, the elemental surface- and near-surface species consist exclusively of Si and C. This indicates that after the IA process the bulk species are preserved.

High resolution XPS data were taken for all the prominent photoelectric peaks observed in the survey to determine the chemical states of Si and C. For both species it was found

that the predominant chemical state originates from SiC bonds. In fact, adventitious C, which is always present on air-exposed substrates, was of a much lower concentration than expected, giving further support to our assertion that the surface after annealing is in a nearly ideal state. Since there is a genuine possibility of elemental Si forming on the crystal surface due to the silane overpressure process, this data is particularly important. Excess Si was present only on the 1400 °C annealed sample despite the silane in Ar mixture flow being reduced. Fortunately for the other annealing temperatures no free Si was observed with XPS at the surface, indicating a near ideal process chemistry. That Si would form on the surface of 1400 °C annealed crystals is also understandable since the melting point of Si at STP is 1410 °C, which is clearly at the IA temperature. Fortunately, SiC crystals may be annealed at 1400 °C in Ar with little surface morphology degradation, as we have also demonstrated in our reactor.

2.5.5. Future Work

An implant annealing process for SiC was developed and found to not only activate the ions but to leave the surface morphology intact. By investigating both n- and p-type implanted epitaxial layers, process stability for either conductivity type was verified and it is believed that the process is robust up to 1600 °C. Annealing conducted at 1700 °C, while not resulting in step bunching, did result in a small amount of pitting, indicating that further process refinement is necessary for this implant temperature. Calculations have been completed to predict the necessary increase in silane flow necessary to achieve a 1700 °C process [26]. A surprising outcome of this research is the observation of nearly ideal surface chemistry after the anneals, which indicates that the anneals may be directly followed by additional epitaxial layer growth, which is of interest for buried structures in some device topologies.

2.5.6. Publications

S. E. Saddow, V. Kumar, T. Isaacs-Smith, J. Williams, A. J. Hsieh, Graves and J. T. Wolan, "Implant Anneal Process for Activating Ion Implanted Regions in SiC Epitaxial Layers," Proceedings of the Korean Institute of Electrical and Electronic Material Engineers (KIEEME), invited paper, to be published in the December 2000 issue.

S. E. Saddow, M. Capano, J. A. Cooper, M. S. Mazzola, J. Williams and J. B. Casady, Mater. Science Forum Vols. 338-342 (2000) pp. 901-904, Trans Tech Publications, Switzerland.

V. Kumar, 'An Implant Annealing process for SiC,' MS Thesis, Mississippi State Univ., May 2001.

2.6. Contacts

A low contact resistance is required in power devices to achieve a high current density in the on-state with a low forward voltage drop. In wide bandgap semiconductors, such as SiC, the reduction of contact resistance to acceptable levels is more difficult than in Si. The main reasons are lower dopant solid solubility, incomplete dopant activation and high work function difference between metal and semiconductor Fermi levels. Consequently, p-type contacts normally exhibit higher contact resistance than n-type contacts, because all the above parameters are less favorable for p-type than n-type. Therefore, p-type contacts in SiC have been the subject of many investigations.

At the beginning of the Megawatt program we recognized the importance of this problem, since it affected all our devices. Although the literature and our own experience provided some guidance in this regard, it was necessary to further reduce the p-type contact resistance with a process compatible with our device structures. Hence, we planned an experiment to evaluate the effect on contact resistance of multiple process variants.

The test mask included circular diodes of various sizes, linear transmission-line-method (TLM) and cross-shaped 4-terminal Kelvin devices for measuring contact resistance, and Van der Pauw structures for measuring the sheet resistance of the top layer. The p-type regions were isolated using mesa etching in the case of a p-type epi layer or selective masking in the case of Al/C co-implantation.

The choice of variants was based on a planar p^+n diode with vertical current flow, as required for power devices. The main variants were: (1) metallization scheme; (2) SiC polytype, i.e. 6H and 4H; (3) p-type doping method, i.e. by epi growth or Al/C co-implantation; (4) p-type doping concentration; (5) contact anneal temperature.

In our standard process we used lift-off to selectively deposit 1700 Å Al and 600 Å Ti over the p-type contacts, followed by annealing at 925 °C for 2 min. Since this temperature is above the Al melting point, the Al layer often segregated into islands during annealing leading to wide variations of contact resistance from run to run. A possible cause was lack of alloying uniformity between Al and SiC, which might originate from excess Al. Therefore, a thinner Al layer appeared to be a potential solution. Two variants were tested, one with 500 Å Al and the other with 1000 Å Al. However this change required a barrier layer, for which Ni was a suitable choice. In this experiment 1000 Å Ni was chosen. To prevent Ni from oxidizing and thus reducing its electrical conductivity, the stack was covered with a very thin (300 Å) Al layer to form a sacrificial oxidation barrier.

The dependence of contact resistance on SiC polytype was another element of this study. It was necessary to determine whether higher contact resistance observed in early 4H experiments was an intrinsic lattice property or the result of a not-yet mature 4H crystal growth technology. Moreover, our past experience was limited to 6H-SiC, because this

polytype is preferable for low-power MOSFETs. Instead, for power devices, 4H is preferred because of higher mobility in the vertical direction along the main current flow.

Another important variant was the method of p-type doping. Etching an Al-doped epi layer to create a mesa p-type region was used conventionally to form SiC p+n diodes. In contrast, our approach was based on a novel Al/C co-implantation technique [27]. The possibility of incomplete Al activation was a major concern, because of the strong dependence of the Schottky barrier height on surface concentration and, likewise, of the contact resistance. Moreover, it was not known the effect of implant damage and of possible "step bunching" due to very high temperature (1600-1700 °C) Al implant activation.

The contact annealing temperature was another important parameter to be investigated. While traditionally we used 925 °C for 2 min, the contact annealing temperature reported in the literature varies from 800 °C to 1100 °C. We chose to investigate three settings, i.e. 800 °C, 925 °C and 950 °C, which were consistent with the rest of the process. This variant created a problem with the execution of the experiment, because in our test mask the testing pads of the TLM and Kelvin structures are formed only after passivation and final metallization. The only devices available for testing after the first metallization were the circular diodes. On the other hand, the number of wafers needed for completing each sample with the remaining process steps would have been prohibitive unless the wafers were cut in pieces before the contact anneals. Our processing group rejected this

Table 2-2. Contact and series resistance (ohm-cm^2) of SiC p+n diodes at 3V

SiC contact formation characteristics				Metallization scheme (from p-type SiC up)					
SiC poly-type	SiC contact region	Nominal surface concent. (at/cm3)	Contact anneal temper.	Al, 1700 Å Ti, 600 Å		Al, 500 Å Ni, 1000 Å Al, 300 Å		Al, 1000 Å Ni, 1000 Å Al, 300 Å	
				Min	Max	Min	Max	Min	Max
6H	Al/C implant	$2x10^{20}$	800 °C	0.01	2.0	1.0	8E+4	1.0	1E+7
6H	Al/C implant	$2x10^{20}$	925 °C	0.01	0.08	0.8	1E+8	0.5	5.0
6H	Al/C implant	$2x10^{20}$	950 °C	0.007	0.015	0.2	200	0.1	5.0
4H	Al/C implant	$2x10^{20}$	800 °C	0.001	0.004	0.002	0.003	0.002	0.005
4H	Al/C implant	$2x10^{20}$	925 °C	0.002	0.003	0.002	0.003	0.002	0.005
4H	Al/C implant	$2x10^{20}$	950 °C	0.002	0.003	0.001	0.003	0.001	0.005
4H	Al-doped epi	$1x10^{19}$	800 °C	0.004	0.1	0.8	1.0	0.5	1.0
4H	Al-doped epi	$1x10^{19}$	925 °C	8E-4	0.004	0.07	0.1	0.02	0.1
4H	Al-doped epi	$1x10^{19}$	950 °C	4E-4	0.001	0.002	0.03	0.002	0.03

option, since it would have been too expensive in terms of processing cost. Therefore, we decided to use sequential anneals of the same wafers at progressively higher temperature with intermediate measurement of the diode forward resistance between anneals.

Table 2-2 shows the results of the intermediate measurements. Since they represent diode forward resistance values, they include many other resistance components besides the p-type contact resistance. Foremost are the n-type substrate series resistance, junction forward resistance and bottom contact resistance. For a 4H-SiC 300 μm-thick n-type wafer doped at 2e17 cm^{-3} these resistance components add to ~ 0.002 ohm-cm^2. Hence, this table only shows if the p-type contact resistance is a dominant factor or not of the total forward diode resistance at the test voltage of 3 V, used for these measurements. Unfortunately, true values of contact resistance are not available from this experiment, because other program priorities prevented the completion of all the measurements.

Among the metallization schemes, the one with the lowest diode resistance for all the process variants is the standard metallization (1700 Å Al / 600 Å Ti). The other two metallization schemes provide an equally low resistance only for the 4H-SiC case with Al/C implant. These resistance values are fully accounted by the the diode resistance components not associated with p-type contact resistance, as estimated above. With the standard metallization the contact anneal temperature is not critical, since the results appear to be independent from this parameter within the experimental range.

Comparing 4H with 6H polytypes, the 6H results are worse and are characterized by a large data spread. Moreover, the influence of the metallization scheme and contact anneal temperature is stronger for 6H, as demonstrated by unacceptably high resistance values for this case, except for the standard metallization and at the highest contact anneal temperature (950 °C). Epi-doping appears to reduce forward diode resistance compared to Al/C implant even for reduced p-type doping concentration, i.e. $1x10^{19}$ vs $2x10^{20}$ cm^{-3}. A plausible explanation is that the extremely high temperature used for Al implant activation leads to loss of Si and possibly also Al near the surface with consequent dopant depletion at the contact interface.

In conclusion, for the standard metallization the p-type contact resistance is not a dominant factor in p+n forward biased diodes measured at 3 V at room temperature. Moreover, for 4H-SiC Al/C implanted diodes, all three metallization schemes yield low resistance values with contact anneal temperatures ranging from 800 to 950 °C.

2.7. Passivation

Proper functioning of power devices requires a suitable passivation scheme to protect the device surface against mechanical and electrical failures. In particular, passivation is needed to isolate high voltage leads and bonds at the chip surface from adjacent low voltage regions, thereby avoiding catastrophic breakdown due to arcing.

In silicon devices passivation techniques have been developed to suit the corresponding device structures and packaging concepts. In our program we simply extended to SiC the Si passivation techniques, ignoring for the time being the differences of device and material characteristics, such as higher operational temperature, different material properties, different metallization and different topology. Therefore, we were not surprised when we discovered during testing that our passivation scheme needs improvements to avoid premature reverse voltage breakdown even in junction-terminated (JTE) devices, especially diodes and GTOs.

Our passivation method consisted of depositing by CVD at 400 °C an SiO_2 layer, 6000 Å thick, after contact metallization. Vias were opened in this layer for connecting the bonding pads with the device top contacts. The bonding pads were formed by depositing a multi-metals stack covered by gold and were patterned using lift-off. This bare minimum passivation is particularly vulnerable to high voltage breakdown, because the dielectric strength of low temperature oxide is only 600 V/μm.

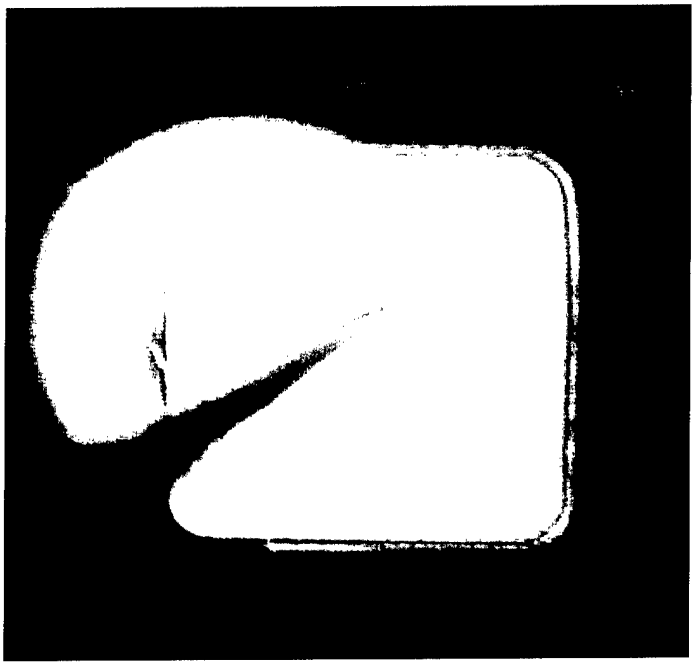


Figure 2-19. Visualization of a breakdown voltage event during wafer probing of a 5000 V PiN diode

At the beginning of the program this was not a problem, because the combination of high defect density and thin epi layers prevented achieving high blocking voltage. Moreover, for wafer probe testing, the passivation properties could be enhanced by applying a polymer layer, called Fluorinert. This allowed us to test our PiN diodes above 5000 V. However, Fluorinert provides only a temporary voltage isolation, as evidenced by the occurrence of breakdown after prolonged voltage application. Figure 2-19 shows a breakdown event in progress on a 5000 V diode, where the starting point is at a corner of the anode. On this picture the breakdown location appears as a large clear circular halo due to light emission caused by arcing. As the phenomenon progresses, the circle expands until a small flash marks the destruction of the device, while simultaneously the device I-V characteristics change from rectifying to a short circuit on a semiconductor tester.

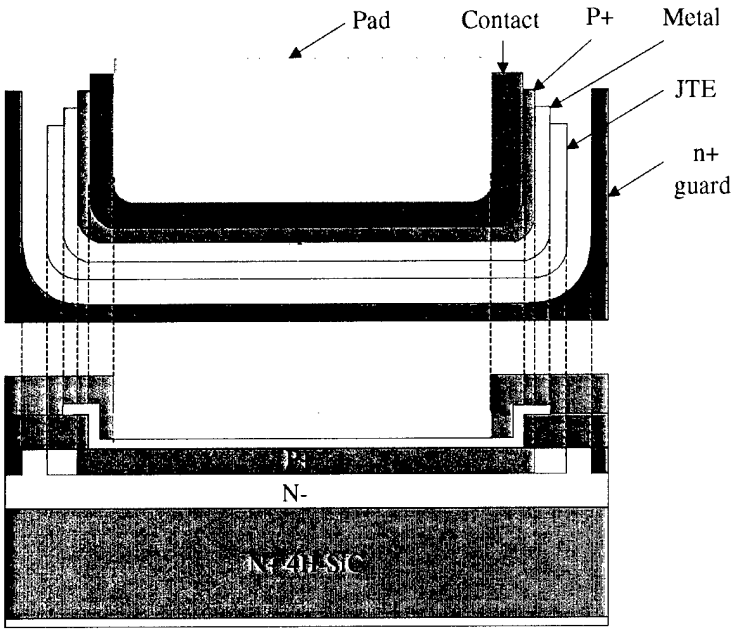


Figure 2-20. Cross-section and layout of planar PiN diodes

An investigation was launched to explain this breakdown phenomenon. Since the diode was designed with a junction termination extension (JTE) and this design was validated with numerical modeling, we could exclude with a high degree of confidence the occurrence of breakdown in SiC. Therefore, we examined the device structure above the SiC surface and its topology to determine if there were regions, where the electric field could exceed the critical value under high voltage stress. Figure 2-20 shows the cross-section and planar view of the tested PiN diodes with the relative position of each level edge.

The first observation is that in planar diodes the top SiC surface consists of P^+, N and N^+ regions. The P+ region forms the anode, while the N+ the guard-ring, which is internally connected to the bottom-side cathode through the N substrate. Hence, both high and ground potentials co-exist on the surface. For avoiding breakdown, the nearest adjacent points between voltage extremes must be distant enough to maintain a sub-critical electric field in the oxide or other overcoating materials. Unfortunately, due to a design error, the metal pad in contact with P+ extends in our diodes over the field oxide, which is about 1 μm thick. Although this extension does not directly overlap the N region, it is too close to it to provide adequate safety for 5000 V. We believe that this is the main source of the breakdown failure observed in Figure 2-19.

After correcting this design error, there is still the problem of the potential distribution around the edges of the anode metal pad. While this distribution is optimized in SiC using a device design CAD, such as MEDICI, it is usually ignored in the film and passivation structure, because this is regarded as an unnecessary complication of the device model. In the future we recommend to specify the passivation scheme from the beginning of the device development and to include it in the numerical simulations to ensure full voltage protection.

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3. Device Physics

Device physics is the core of the SiC Megawatt program. At the beginning of the program the feasibility of many types of power devices has already been established. However, these devices were developed using older process technology in an exploratory mode without focusing on manufacturability and reliability. The main objective of the SiC Megawatt program was to move forward in device physics and engineering toward development of prototype devices for transfer to manufacturing.

To accomplish this mandate we used a systematic device development plan, similar to that employed for Si power devices. We started with an initial review of alternative device structures to evaluate their compliance with process technology capabilities and SiC material properties. The selected structure was then numerically simulated using an enhanced version of the MEDICI 2-D modeling program with accurately chosen SiC material parameters. The static and dynamic device performance was predicted through a series of modeling iterations, which led to the choice of optimal device parameters. A process sequence was then formulated and used to generate a set of design rules. A mask set was laid out including device design variants and various test elements for process diagnostic purpose. After a separate development of the most challenging portions of the process, two full lots were fabricated for generating enough wafers for a thorough evaluation and for incorporating in the second lot the revisions suggested by the test results of the first lot. The best dies identified during wafer probing were diced and packaged for functional testing.

Our development effort focused on five types of power devices, which reached various level of completion: (1) 500 V Schottky diodes; (2) 5000 V PiN diodes; (3) 5000 V GTO; (4) 100 V DIMOS FETs; (5) 5000 V MOS-gated Bipolar Transistors (MGT). As mentioned earlier, SiC MOS fundamental problems, which the entire SiC community shares, negatively affected the development of the last two devices. On the other hand, excellent results were achieved on bipolar devices, especially diodes, which led to a further increase of efforts in this direction to accelerate their transfer to production.

For each device a short introduction sets the stage for describing the development effort. The purpose of this introduction is to discuss the main characteristics of the device in a SiC environment and to properly assess its current position in the learning path. The design section justifies the approach selected for implementing the device in SiC. The modeling section presents the results of analytical and numerical modeling performed to optimize the process parameters in relation to the electrical specifications. The fabrication section illustrates the process sequence with device cross-sections at critical process stages. Finally, test results are presented for static characteristics and switching waveforms. The objective of this review is to transfer the technology developed during the program to the SiC device community by providing a detailed and systematic description of our device development effort and our learning experience.

3.1. PiN diodes

The SiC Megawatt program required PiN diodes to provide a flyback return path in the half-bridge circuit. In this regard the main advantage of SiC PiN diodes is their capability of blocking a very high voltage (5000 V) with low leakage current even at high temperature and of switching at high frequency with low power loss. These properties are uniquely possessed by SiC PiN diodes, since SiC Schottky diodes exhibit higher leakage current at high blocking voltage with strong temperature dependence.

High voltage SiC PiN diodes with 6.2 kV and 12.3 kV breakdown voltage have been reported using the mesa approach [1,2] and with 3 kV using the planar approach [3]. The mesa approach has been preferred in the past, because after the epitaxial pn junction only few processing steps are needed to complete the device fabrication. However, as the voltage rating increase, the junction termination becomes an important factor for reaching consistently a high breakdown voltage. In mesa structures the junction termination requires multiple SiC trench etching steps with accurate depth calibration, controlled profile slope and smooth surface morphology, both on the sidewalls and at the bottom. These properties are affected by interactions of the etching method with the epi surface morphology and crystal defects, leading to variations within wafers and from lot to lot. This problem is especially troublesome for device fabricators that depend on purchased epi wafers, because they cannot control entirely the critical pn junction formation and the junction termination steps. These reasons played a key role in a trend shift toward planar fully implanted SiC PiN diodes. Moreover, planar implanted diodes are considered more manufacturable, cheaper to produce, and more consistent with industrial separation between epi wafer supplier and device manufacturer.

In agreement with this trend we selected the planar implanted approach, for which we could also draw from our pioneering work on ion implantation in SiC [4,5]. Our goal was to develop a high yield process that could be adjusted for a wide range of blocking voltage ratings with minor mask and implant dose modifications. Accordingly, the junction termination extension (JTE) was also fully implanted like the anode using a similar energy range. The fabricated diodes achieved a blocking voltage of up to 4.5 kV using 40 µm epi [6], which at that time was the highest reported blocking voltage for an implanted junction rectifier in SiC. Later, using this process and 70 µm epi, the blocking voltage rose in excess of 6 kV and was limited by the passivation dielectric strength.

3.1.1. Design

We designed a 5 KV implanted SiC PiN diode by choosing a device structure compatible with the material properties, implant technology and ease of manufacturing, and also capable of meeting the diode electrical specifications. The selected structure is shown in Figure 3-1.

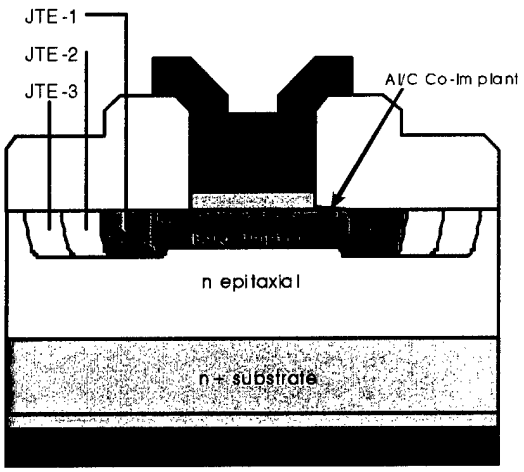


Figure 3-1. Implanted SiC PiN structure

The high mobility ratio between electrons and holes in SiC (10:1) left no choice but to use an N^+ substrate and N^- drift region. Otherwise, the vertical resistance of these thick regions would have severely limited the forward conduction and caused a high power loss. This explains the popularity of p+n power diodes in SiC, despite the fact that, contrary to Si, the holes ionization coefficient in 4H-SiC is higher than that of electrons, thereby reducing the breakdown voltage. As it is now common for SiC power devices, we selected the 4H polytype, because of higher mobility in the vertical direction than the 6H crystal.

For a 5000 V diode, we preferred to use a punch-through (PT) structure to support the reverse voltage. In this case, the electric field varies more gradually with distance in the drift region due to a lower doping concentration of the lightly doped N^- epi layer. Moreover, a thinner epi is sufficient compared to the non-punchthrough (NPT) case because of the lower doping concentration. Consequently, the starting material will cost less. Finally, because of the reduced drift layer thickness, its ohmic resistance is smaller in the PT structure than in the NPT one with the same blocking voltage.

Figure 3-2 shows a graph of breakdown voltage versus doping concentration in SiC for the PT structure. This graph shows that a 40 μm thick epi doped to $2x10^{15}$ cm^{-3} is adequate to provide a plane junction breakdown voltage of 5000 V. We used 12 μm, 40 μm and 70 μm epi layers with a doping concentration as low as possible in the range $6x10^{14}$-$2x10^{15}$ cm^{-3}. Although 40 μm is the theoretical drift region thickness for a 5 KV breakdown voltage at this doping level, the other two values were used for reducing the development cost (12 μm) and for increasing the parametric yield of the breakdown voltage (70 μm).

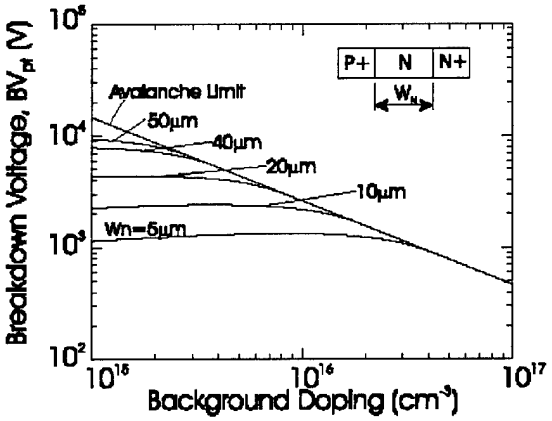


Figure 3-2. Breakdown voltage of SiC diodes versus doping concentration and epi layer thickness for punchthrough (PT) design

Table 3-1 provides a summary of the implant conditions used for the PiN diodes. We used a 3-zone junction termination extension (JTE) to prevent premature peripheral breakdown with respect to the plane area bulk value. The 3 zones, named JTE1, JTE2 and JTE3, have progressively larger width

Table 3-1. Implants for PiN SiC diode

- Drift Layer Thickness: 12 m, 40 m, 70 m
- Drift Layer Doping: 6×10^{14} - 2×10^{15} cm^{-3}
- Boron Implants for JTE:
  - JTE-1: 25 KeV-300 KeV, 1.9e13 cm^{-2}, 650 C
  - JTE-2: 25 KeV-300 KeV, 1.2e13 cm^{-2}, 650 C
  - JTE-3: 25 KeV-300 KeV, 6.6e12 cm^{-2}, 650 C
- Boron Implant Emitter: Box, 3.3e14 cm^{-2}, 650 C
  25 KeV to 300 KeV
- Al/C Co-implanted shallow layer:
  - Aluminum: 30 KeV-180 KeV, 3.6e15 cm^{-2}, 800 C
  - Carbon: 30 KeV-120 KeV, 3.0e15 cm^{-2}, 800 C
- Nitrogen Channel Stop: Box, 5.0e15 cm^{-2}, 650 C
  25 KeV to 300 KeV
- Anneal cycle: 1650 °C, 45 min, argon
- Breakdown Voltage: 1100 V - 6000 V

and smaller boron implant dose, as shown in Figure 3-1 and Table 3-1. The width and dose of the JTE regions were adjusted with 2-D numerical simulations in order to minimize the electric field at the periphery below 1 MV/cm.

The anode design employed a combination of boron, aluminum and carbon implants. The boron implant energy was calculated using SUPREM aiming for a junction depth of 0.65 μm, which is similar to the JTE implant range. Utilizing contact resistance results reported in section 2, we co-implanted shallow Al and C to lower the Schottky contact barrier. In addition, we used an N^+ channel stop along the die outer edge to neutralize the electric field along the scribe lanes for passivation purpose.

Although implant activation requirements vary from one species to another, we decided to merge all the anneals into one to reduce the amount of Si evaporation and related damage due to step bunching. The annealing conditions were chosen to satisfy those of boron (45 min in argon at 1650 °C), because, since they were the most demanding, they would also satisfy those of the other dopants.

3.1.2. Modeling

Since the PiN diode is the basic bipolar device, it requires an accurate model that can be used as a building block for modeling other bipolar power devices, including BJT, GTO and IGBT. Prof. T.P. Chow and his team at RPI have devoted a large effort to the development of a complete physical model of the SiC PiN diode using analytical formulas. Diodes fabricated with the support of various programs, including the SiC Megawatt program, allowed for comparison of test results with modeling predictions, thereby improving both the model and the diode design.

Before this work, widely used 2-D numerical simulators, like MEDICI, displayed many shortcomings in predicting PiN static and dynamic electrical characteristics. These were caused by various factors that complicate device modeling in SiC. One such factor is the existence of multiple defect levels in a wide energy bandgap [7]. Another one is the partial carrier freeze-out at room temperature due to deep dopant energy levels. These changes in semiconductor properties had to be accounted by modifying the classical Shocley-Noyce-Sah theory in order to obtain a useful diode model [8]. Working together with companies that produce and support numerical device simulators, the RPI team has

transferred this knowledge to the SiC community leading to improvements in simulator programs, such as MEDICI.

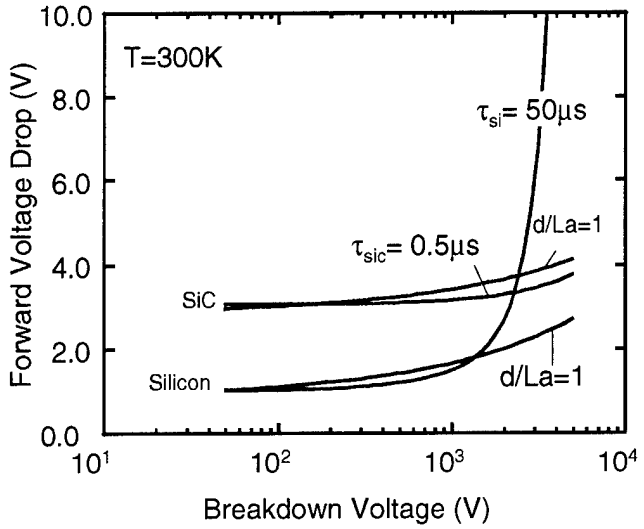


Figure 3-3. Forward voltage drop versus breakdown voltage as a function of carrier lifetime for Si and SiC rectifiers. d/La is the ratio of one half of the drift region thickness to the ambipolar diffusion length.

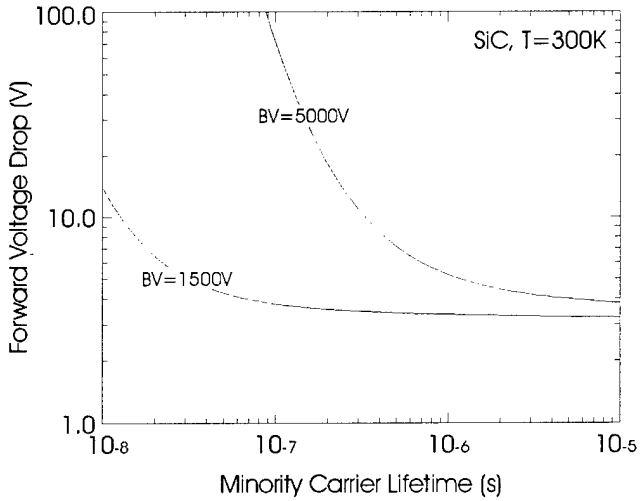


Figure 3-4. Simulated forward voltage drop dependence on minority carrier lifetime of 4H-SiC PiN diodes with 1500 V and 5000 V breakdown voltage at 100 A/cm^2 and 300 K

The challenge of PiN diode modeling consists in simulating with high accuracy the forward I-V characteristics, especially the forward voltage drop and current density at various temperatures, and the switching behavior. On the other hand, modeling of the reverse characteristics is not as critical for the diode designer, because the breakdown voltage dependence on drift region properties is straightforward and the reverse leakage current is too dependent on the crystal defects to be worth modeling for diode design purpose.

A key objective of the PiN power diode designer is to achieve for a given blocking voltage the lowest forward voltage drop at a given current density and temperature with the fastest switching speed. Modeling is necessary to optimize the trade-off among these conflicting requirements. As the blocking voltage increases, the drift region becomes thicker and more lightly doped. This also leads to an increase of the specific on-resistance and consequently higher forward voltage drop. One reason for the selection of SiC for high voltage devices is that the higher critical electric field of SiC compared to Si allows to support the blocking voltage with a thinner and more heavily doped drift region. Therefore, when the forward bias is applied, the on-resistance is significantly decreased.

One aspect of the on-resistance versus breakdown voltage relationship, which is often neglected, is the impact of the carrier lifetime, τ_a, on this relationship. The physical diode model shows that optimal conductivity modulation occurs when the ratio of half drift region thickness to ambipolar diffusion length, d/L_a, is close to 1. Since d increases with blocking voltage, L_a must increase at the same rate to keep the ratio constant. In high voltage Si diodes this leads to slow switching devices, because τ_a grows with the square of L_a. Fortunately, in SiC d can be much smaller because of the high critical electric field allowing L_a and τ_a to be small while the diode operates in conductivity modulation. Figure 3-3 shows the simulated forward voltage drop versus blocking voltage as a function of ambipolar carrier lifetime in Si and SiC. Notice that for a 5000 V Si diode with a 50 μs lifetime the forward voltage drop, V_f, is unacceptably high above 8 V due to a sharp increase of this parameter with blocking voltage as it approaches the 5000 V mark. This contrasts with a 5000 V SiC diode, for which V_f is less than 4 V even with a τ_a of 0.5 μs and only slightly higher than the V_f value at 100 V with the same τ_a.

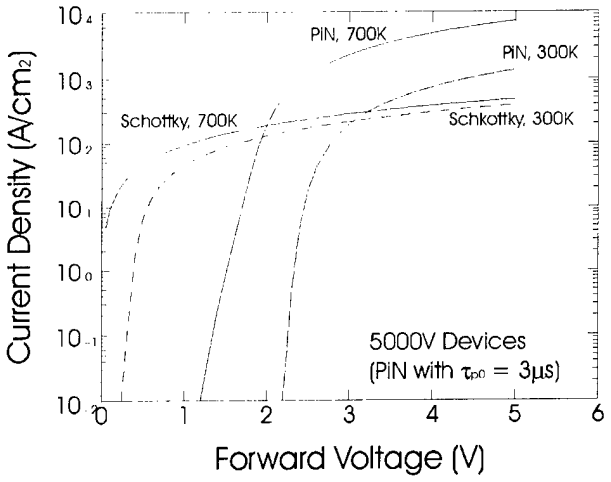


Figure 3-5. Simulated forward I-V curves of 5000 V SiC PiN and Schottky rectifiers at 300 K and 700 K with a lifetime of 3.0 μs

Since our goal is to design a 5000 V PiN diode, the model was applied to determine the minimum lifetime required to achieve an acceptable forward voltage drop for this device. This could be extracted from Figure 3-4, which plots V_f versus τ_a for SiC diodes with breakdown voltages of 1500 V and 5000 V at 300 K. This figure shows that for a 5000 V diode a $\tau_a > 1$ μs is necessary to achieve V_f (at 100 A/cm^2) < 5 V. Unfortunately, the control of the starting material lifetime in SiC is outside the realm of the device fabricator. After a future reduction of defect density and a corresponding increase of carrier lifetime, the device fabricator will be able to adjust the lifetime to a design target using high-energy irradiation, as done for Si. Until that time, this model shows that the forward drop of PiN diodes and hence the on-resistance will be strongly dependent on the material properties and reflect their starting material lifetime variation. Figure 3-4 has also been used for diagnostics since it allows to estimate the lifetime from measurements of forward voltage drop on fabricated diodes. This technique was applied by Cree on some occasions to characterize and improve the epi layer properties.

After choosing a technically feasible value of τ_a the model can predict the I-V curves for various breakdown voltage and temperature values. Figure 3-5 shows simulated forward I-V curves of 5000 V SiC PiN and Schottky rectifiers at 300 K and 700 K using a lifetime

of 3 μs. Notice the significant decrease of forward voltage drop with increasing temperature, especially for the PiN diode.

In addition to the PiN junction model, there are many parasitic effects that need to be accounted for to make accurate predictions. A very important parameter is the contact resistance, which is more severe for the anode contact. As mentioned elsewhere, the substrate ohmic resistance is also a limiting factor on the maximum current density. Finally, the design of the Junction Termination Extension must also be optimized with accurate modeling. The RPI team addressed each of these modeling efforts for the PiN diodes to yield an optimal design. The methodology used and the modeling equations were published in various conference proceedings and refereed journals, but the most detailed description is in Dr. Ramungul PhD thesis [9].

3.1.3. Layout

The main layout features of the 5000 V planar PiN diodes are as follows:

1. Design target of PiN diode with 3-zone JTE and n+ channel stop:
   5000 V blocking capability with peak surface field < 1.0 MV/cm and
   average surface field across JTE < 0.7 MV/cm.

2. Input parameters for design simulation with reference to the main diode cross-section shown in Figure 3-6:
   P-base doping (active acceptors)= 1.2e17 cm^{-3}
   N^- drift layer thickness = 40 μm
   N^- drift layer doping = 2e15 cm^{-3}
   P^+ junction depth = 0.3 μm
   P^+ average concentration = 1e18 cm^{-3}
   N^+ average concentration = 1e19 cm^{-3}
   Contact resistance to P^+ and N^+ = 10^{-5} ohm-cm^2
   JTE zone ratio: W_1:W_2:W_3 = 1:2:1, where W_1=20 μm
   Anode width, W_d = 50 μm

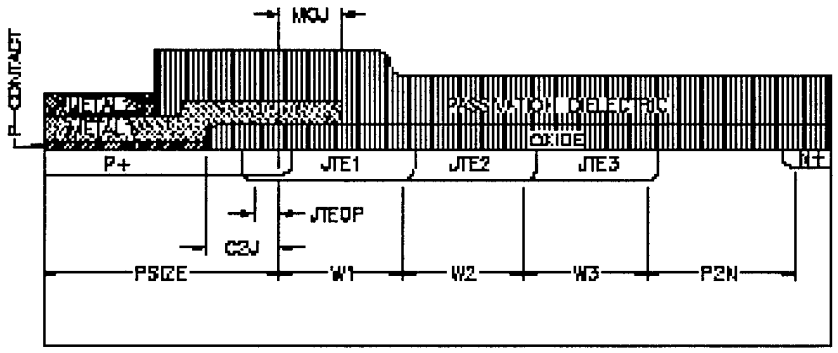


Figure 3-6. Cross-section of main PiN diode

3. Simulated results:

Forward drop, V_f (100 A/cm^2) = 4.5 - 5.0 V for τ_p = 5 μs
Forward drop, V_f (250 A/cm^2) = 5.0 - 5.5 V for τ_p = 5 μs
Forward drop, V_f (100 A/cm^2) = 4.0 - 4.5 V for τ_p = 10 μs
Forward drop, V_f (250 A/cm^2) = 4.5 - 5.0 V for τ_p = 10 μs

4. Masking Layer Assignments:

Step No.	GDS Layer No.	GDS Layer Name	Digitize Data	Purpose
0	0	ALIGN	Clear	Alignment Marks
1	1	PPLUS	Clear	Define anode P^+ implant region
2	2	NPLUS	Clear	Define channel-stop N^+ implant region
3	3	JTE1	Clear	Define JTE1 P^- implant region
4	4	JTE2	Clear	Define JTE2 P^- implant region
5	5	JTE3	Clear	Define JTE3 P^- implant region
6	6	PCONTACT	Clear	Open contact window to P^+ region
7	7	METAL	Dark	Define anode metal pad
8	8	PAD	Clear	Open anode pad window

5. PiN mask set variations

The PiN mask set contains an array of diodes with 3 sizes as shown in the table below. The current rating was calculated assuming a current density of 250 A/cm^2.

Item	Name	Dimension	Junction area	Periphery	Current rating
1	D-300	300 μm x 300 μm	8.10 x 10^{-4} cm^2	1030 μm	0.25 A
1	D-800	800 μm x 800 μm	6.31 x 10^{-3} cm^2	3030 μm	1.5 A
1	D-4000	4000 μm x 4000 μm	16.00 x10^{-2} cm^2	15830 μm	0.25 A

We chose 3 diode sizes for the following reasons. First, we needed an adequate diode yield to draw statistically valid conclusions from process development variants. Second, we wanted to ensure the successful fabrication of a large number of functional devices despite the uncertainty on the starting material defect density. Third, we needed at least few reasonably large diodes with high current rating for power circuit development. Fourth, we wanted multiple sizes to verify a linear dependence of current rating on anode area and to analyze any deviation from this law.

While the largest diode was laid out as a single unit, the medium and small diodes were clustered in arrays of 4 and 16 diodes, respectively. Figures 3-7, 3-8 and 3-9 show the layout of the various diodes, while Figure 3-10 shows a picture of a patterned wafer to indicate the position of the various diodes. One can see that the large diodes are placed near the center of the wafer to maximize their yield assuming that the defect density will

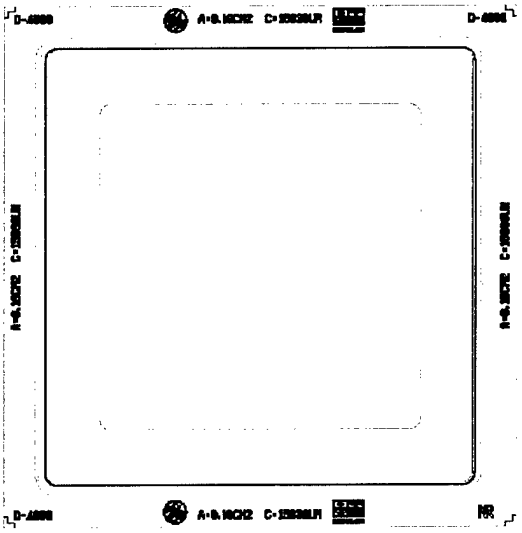


Figure 3-7. Layout of single large 4 mm x 4 mm diode

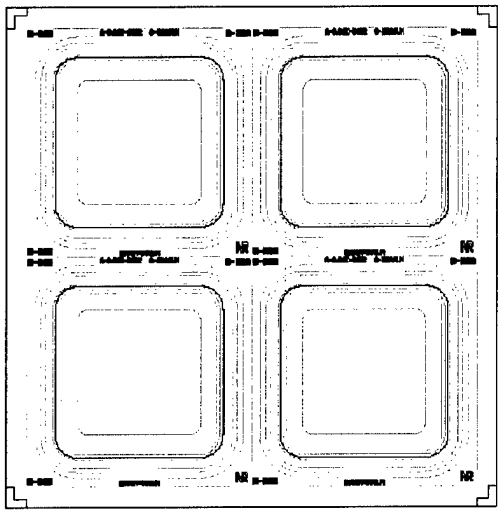


Figure 3-8. Layout of 4 medium 800 µm x 800 µm diode array

be smaller in that region. At the other extreme, the smaller diodes are placed near the periphery, where the probability of defects is higher.

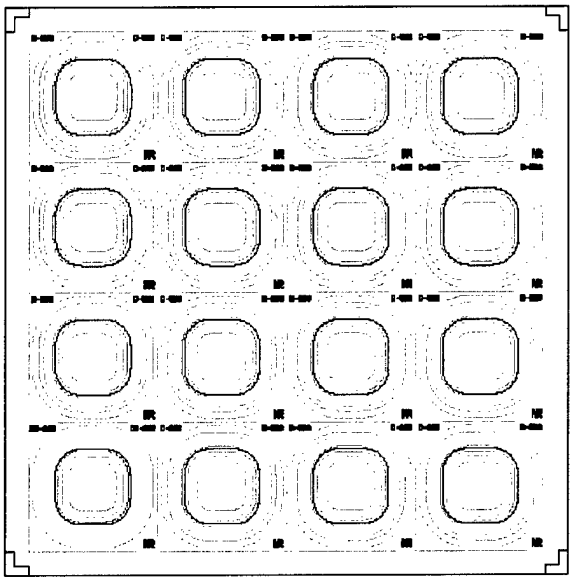


Figure 3-9. Layout of 16 small 300 µm x 300 µm diode array

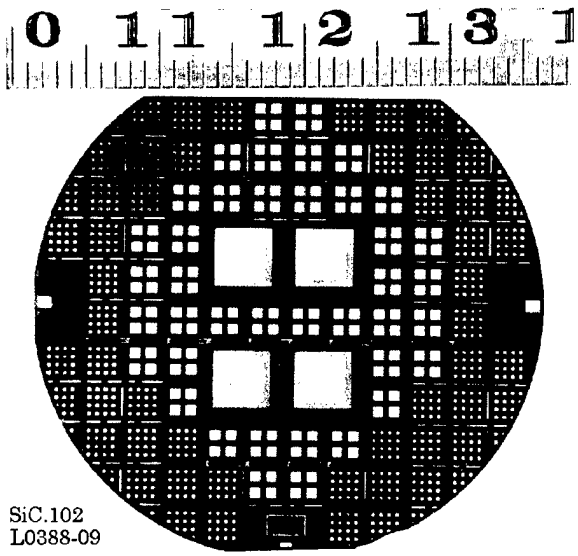


Figure 3-10. Wafer patterned with PiN maskset

6. Electrical Test Element Group

A test element group (TEG) was included in the mask set for process diagnostic purpose. The TEG elements were designed to measure individual device characteristics, which are integrated in the PiN diode, and therefore inaccessible as separate parameters. This

information permits to analyze the PiN diode performance in terms of modeling predictions by adjusting the simulation parameters to realistic process control data.

Item	TEG Group	Description	Purpose
1	TEG1	Van der Pauw resistor	Measure sheet resistance of implanted layers
2	TEG2, TEG4, TEG5	Junction capacitor	Extract doping concentration, generation and recombination lifetime, surface recombination velocity, etc.
3	TEG3	Kelvin 4-terminal contact	Measure contact resistance
4	TEG6, TEG7, TEG8, D-300B, D-300C	JTE	Examine JTE characteristics
5	TEG9	Hall effect mobility	Measure majority carrier mobility, doping compensation ratio, etc. of implanted layers
6	SEM	DEKTAK	RIE characterization
7	SEM	SEM line and space	
8	D-300A	Devices without JTE termination	Monitor the efficiency of JTE termination

3.1.4. Fabrication

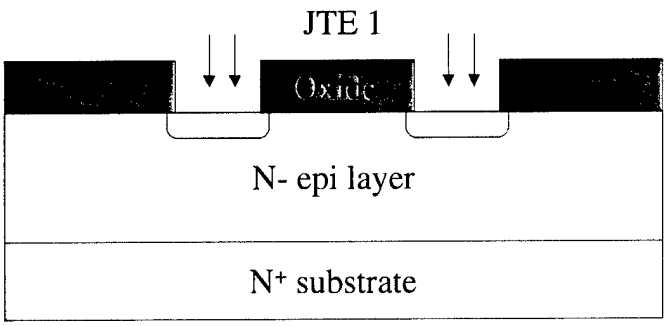
These diodes were fabricated on high-grade 4H-SiC epi wafers produced by Cree. The N^+ substrate had a donor concentration $N_D = 8.6x10^{18}$ cm^{-3} and a thickness of 430 μm. The N^- epi had a donor concentration $N_D = 1.0x10^{15}$ cm^{-3} and measured 12 μm, 40 μm and 70 μm in three successive lots, respectively. The use of multiple epi layer thickness was motivated by the need to minimize wafer cost during development, while at the same time to evaluate the effect of thickness on epi quality and parametric yield. Theoretically, a 40 μm drift layer should exhibit a breakdown voltage of 6.4 kV, but in reality various material defects reduce this value and the corresponding yield. Hence, a larger epi thickness can be used to compensate for yield loss due to blocking voltage, but at the cost of higher on-resistance and wafer expense.

The fabrication process is illustrated in Figure 3-11 using diode cross-sections and an outline of key process steps. A three zone boron implanted junction termination extension (JTE) was used with implanted dose of $1.9x10^{13}$ cm^{-2}, $1.2x10^{13}cm^{-2}$ and $6.6x10^{12}$ cm^{-2} from the inner zone to the outer zone, respectively. The implant energy ranged from 25 to 300 KeV. Doubly charged ions were used for the highest energy implants to overcome the voltage limitation of a medium energy machine. The width of zones 1, 2, and 3 was 20 μm, 40 μm and 20 μm, respectively.

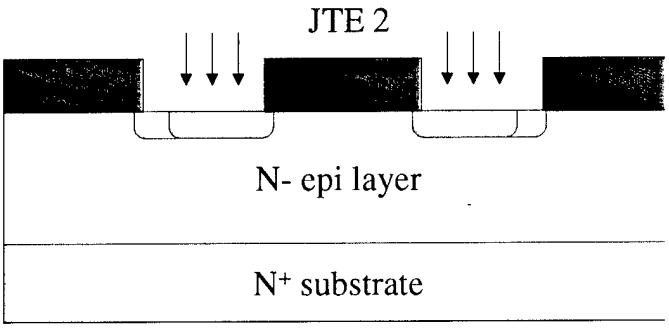
The p^+ anode was formed by deep boron implants and by shallow aluminum and carbon implants. Boron was chosen to minimize junction leakage, while the purpose of the aluminum/carbon implant was to enhance emitter injection and form a low-resistance

ohmic contact. Boron was implanted with energies ranging from 25 to 300 keV at 650 °C with a total dose of $3.3x10^{14}$ cm^{-2} resulting in a junction depth of 0.7 µm. Aluminum and carbon were implanted at 800 °C to a depth of 0.2 µm with energies of 30 - 180 keV for Al and 20 - 120 keV for C, each with a dose of $3.6x10^{15}$ cm^{-2} to achieve an average concentration of $2x10^{20}$ cm^{-3} near the surface. A nitrogen implanted N^+ field stop provides isolation among adjacent devices. All the implants were annealed simultaneously at 1650 °C for 45 min in argon using a SiC cover wafer to prevent Si evaporation.

The top contact to the anode was formed using an Al/Ti metal stack and a lift-off process, while the contact to the backside used Ni. The contacts were annealed at 950 °C for 2 min in a furnace. The top metal consisted of sputtered Ti/Mo. A low-temperature oxide passivating layer was deposited and vias were opened to form a gold bonding pad for the anode. Ti/Pt/Au was sputtered on the backside to provide a metallization suitable for die bonding and an effective ohmic contact for the cathode.

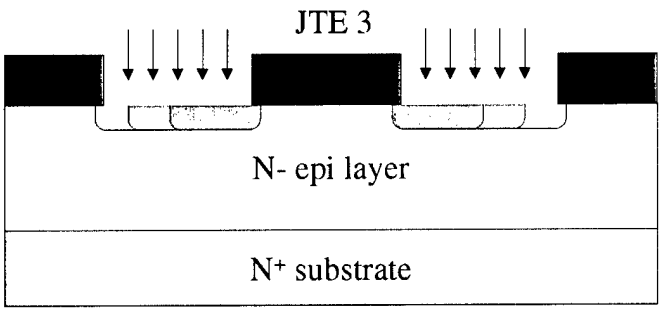


Alignment Marks
Deposit HTO oxide
Sputter aluminum
Pattern with ALIGN mask
Etch aluminum
Strip resist
RIE etch oxide and SIC
Strip aluminum and oxide



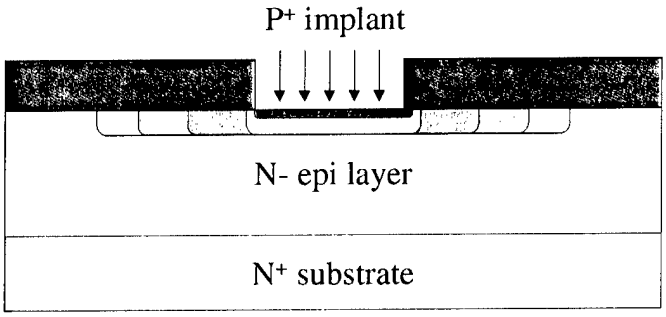
Junction Termination (JTE 1)
Deposit HTO oxide
Pattern with JTE 1 mask
Etch oxide
Strip resist
Implant boron at 650 °C with JTE 1 dose
Strip oxide

Junction Termination (JTE 2)
(like JTE 1 with mask and dose change)

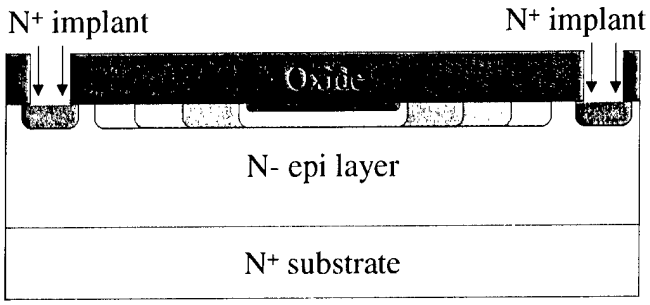


Junction Termination (JTE 3)
(like JTE 1 with mask and dose change)

Figure 3-11a. PiN diode process flow

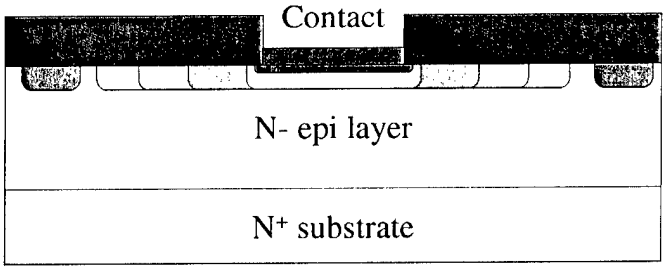


P+ implant
Deposit HTO oxide
Pattern with PPLUS mask
Etch oxide
Strip resist
Implant deep boron at 650 °C
Implant shallow Al and C at 800 °C
Strip oxide

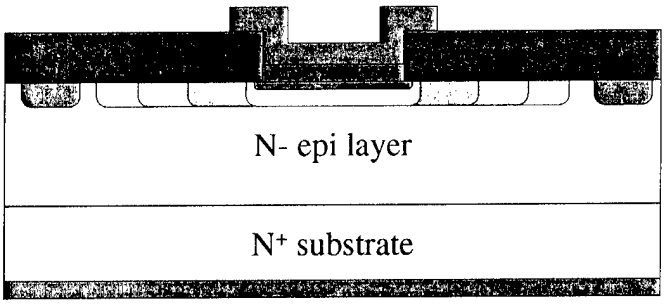


N+ implant
Deposit HTO oxide
Pattern with NPLUS mask
Etch oxide
Strip resist
Implant nitrogen at 1000 °C
Strip oxide

Anneal all implants at 1650 °C



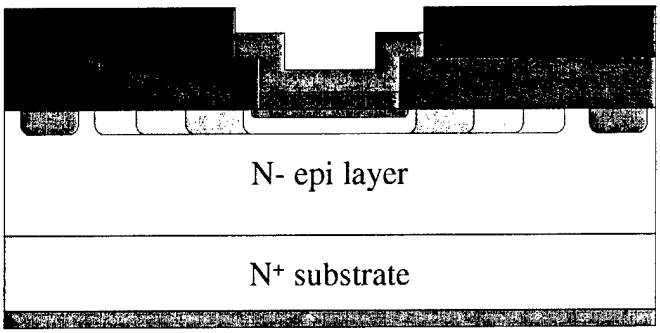
P+ contact
Deposit HTO oxide
Pattern with CONTACT mask
Etch oxide with undercut
Sputter contact metal
Lift-off
Clean residual resist



Backside N+ contact
Protect front with resist
Sputter backside contact metal
Strip resist
Anneal contacts at 950 °C

Top metal
Sputter Ti/Mo layers
Pattern with METAL mask
Etch metal
Strip resist

Figure 3-11b. PiN diode process flow



Passivation
Deposit LTO oxide
Pattern with PAD mask
Etch LTO oxide over metal pad
Strip resist
Sputter backside final metal layers

Figure 3-11c. PiN diode process flow

3.1.5. Static Test Results

Static electrical measurements were performed on unpackaged PiN diodes with epi layer thickness of 12 μm, 40 μm and 70 μm. Typical I-V characteristics were obtained from diodes with 40 μm epi, while breakdown voltage and forward voltage drop histograms and wafer maps were generated from diodes with 70 μm epi.

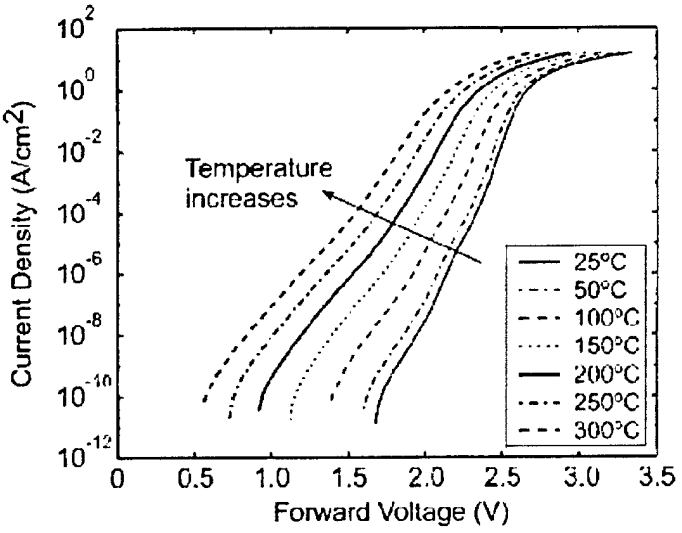


Figure 3-12. Forward I-V characteristics measured between 25 °C and 300 °C of a 4H-SiC implanted PiN diode with junction area of 6.31×10^{-3} cm^2

Figure 3-12 shows the forward I–V characteristics of a typical PiN diode with a blocking voltage greater than 4 kV and a junction area of 6.31×10^{-3} cm^2. Two distinct exponential regions can be observed. In the region from 10^{-4} to 1 A/cm^2, an ideality factor of 1.2 is found over the temperature range from 25 °C to 300 °C. This result agrees well with a generalized Shockley–Noyce–Sah (SNS) model [9], which assumes multiple shallow, s, and deep, d, recombination levels [10]. The ideality factor, n, is then given by n=(s+2d)/(s+d)=1.2, because in this case s=4 and d=1. The activation energy in this region is found to be 2.78 eV, which is in good agreement with the theoretical value of Eg/n = 3.26 eV/1.2. In the second exponential region, below 10^{-4} A/cm^2 , the ideality factor ranges from 1.6 to 2.2 from 25 °C to 300 °C. In this ultra-low-level injection region, the characteristics follow the conventional single deep level SNS model. An activation energy of 1.31 eV is observed in this region.

Forward current–voltage measurements at current densities up to 700 A/cm^2 were made on a Tektronix 370A curve tracer using a 4-probes Kelvin configuration to remove

parasitic series resistance. The on-state voltage of a typical device at 100 A/cm^2 was 4.2 V at room temperature and decreased to 3.3 V at 250 °C mainly due to reduced built-in voltage and increased carrier lifetime at elevated temperatures. The differential series resistance of a typical 800 µm x 800 µm PiN diode was determined using the method of Schroder [10] above 500 A/cm^2. The specific on-resistance measured 2.75 ohm-cm^2 at 25 °C and 2.35 ohm-cm^2 at 250 °C, respectively. This temperature effect is attributed to a contact resistance reduction and conductivity modulation increase with increasing temperature.

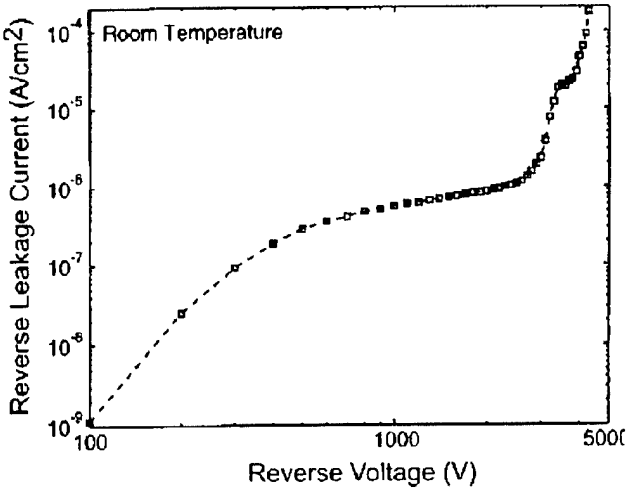


Figure 3-13. Reverse I-V characteristics at 25 °C of a 4H-SiC implanted PiN diode with a junction area of 6.31x10^{-3} cm^2

The reverse blocking characteristics were measured at room temperature under a fluorinert cover to protect against arcing. Figure 3-13 shows typical reverse I-V characteristics of these diodes as plotted on a log–log scale. 16 percent of the 80 units tested blocked up to 4.5 kV with reverse leakage current less than 1µA. Unfortunately, these diodes self-destructed during high-voltage testing when the current exceeded 10 µA. The reverse leakage current obeys a square-root dependence for reverse voltages between 500 V and 1500 V as predicted by space-charge generation theory. Above 1500 V, the drift layer is fully depleted and the leakage current increases faster than $V^{1/2}$ in this region. Even below the punchthrough voltage, the magnitude of the reverse leakage current is much larger than the contributions from diffusion, bulk space-charge generation or perimeter generation. To account for the measured leakage current an incredibly small bulk generation lifetime on the order of 10^{-23} s or a surface recombination velocity of approximately $3x10^{21}$ cm/s would be necessary. Both of these values are unlikely and some other mechanism, such as dislocations or other defects, must account for the observed leakage current.

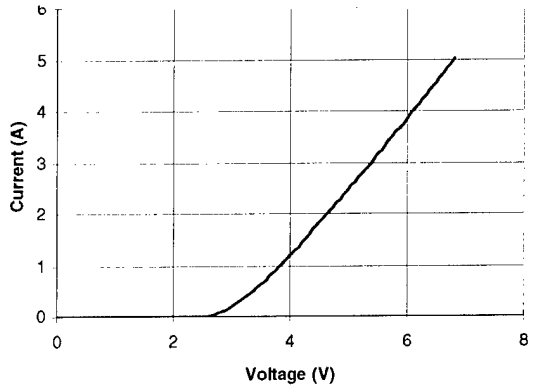


Figure 3-14. Forward I-V curve measured at 25 °C of large SiC PiN diode with junction area of 0.16 cm^2 and 40 µm epi. V_f=6.82 V @ I_f=5 A, J=31.25 A/cm^2

The forward characteristics used for evaluating the device model are usually plotted on semi-log graphs to extract the power law relationship for various ranges of current density, as shown in Figure 3-12. On the other hand, for power circuit

applications, a key measurement of technology capability is the forward current rating for a given voltage. Figure 3-14 demonstrates a 5 A capability at a forward voltage drop, Vf = 6.82 V, for implanted PiN diodes with a junction area of 0.16 cm^2, built in 1998 at GE CRD as part of this program. These measurements were made on unpackaged diodes at 25 °C without compensating for series resistance. Although this result was encouraging, we clearly recognized the limitations on current rating imposed by the defect density of the starting material. This acts in two ways: (1) by placing a ceiling on the diode size to achieve a reasonable yield; (2) by lowering the carrier lifetime with consequent decrease of conductivity modulation. However, these effects are transitory and as the SiC technology will evolve the diode current rating and voltage forward drop will asymptotically trend toward the theoretical values for a given junction area and blocking voltage.

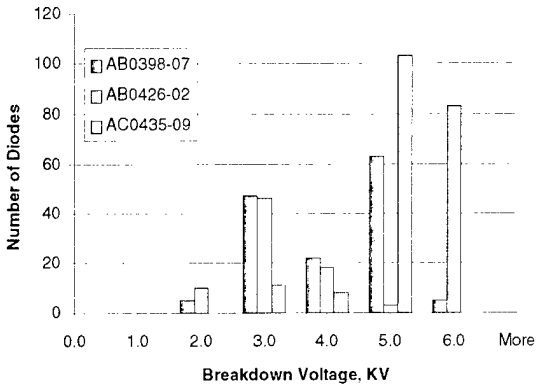


Figure 3-15. Histogram of breakdown voltage measured at 200 µA and 25 °C for SiC PiN diode with junction area of $6.4x10^{-3}$ cm^2 and 70 µm epi

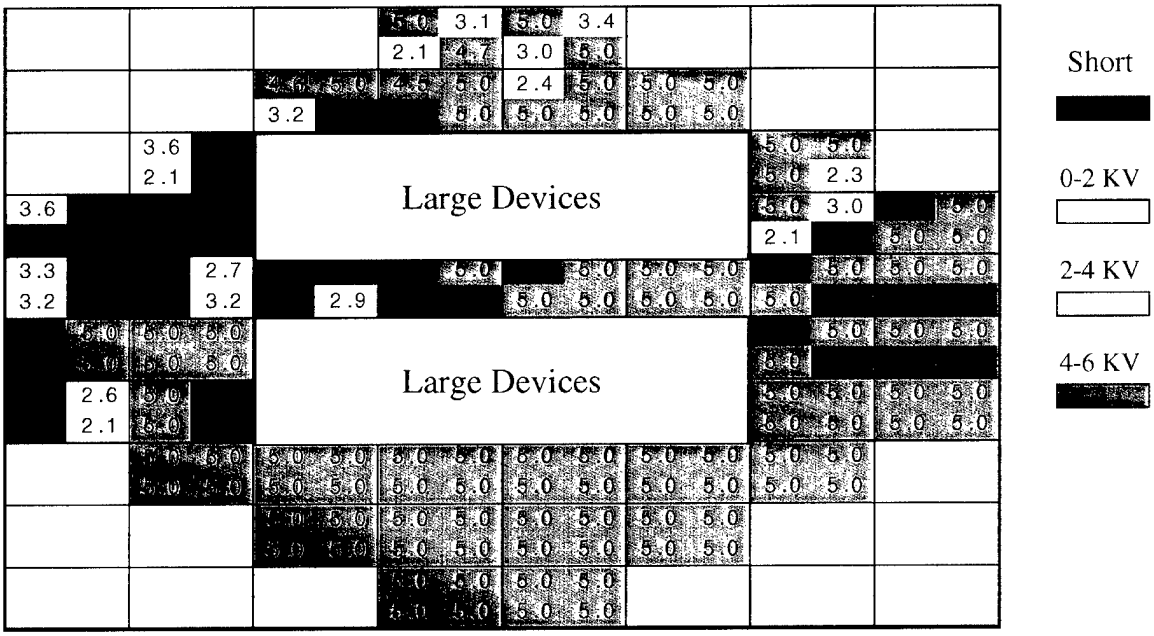


Figure 3-16. Wafer map of breakdown voltage, BV, measured in KV at 200 µA and 25 °C for SiC PiN diodes with junction area of $6.4x10^{-3}$ cm^2 and 70 µm epi. Every cell shows the corresponding BV value.

The diodes built on 70 µm epi provided interesting statistical results with regard to the parametric and spatial distribution of the breakdown voltage, BV, reverse leakage

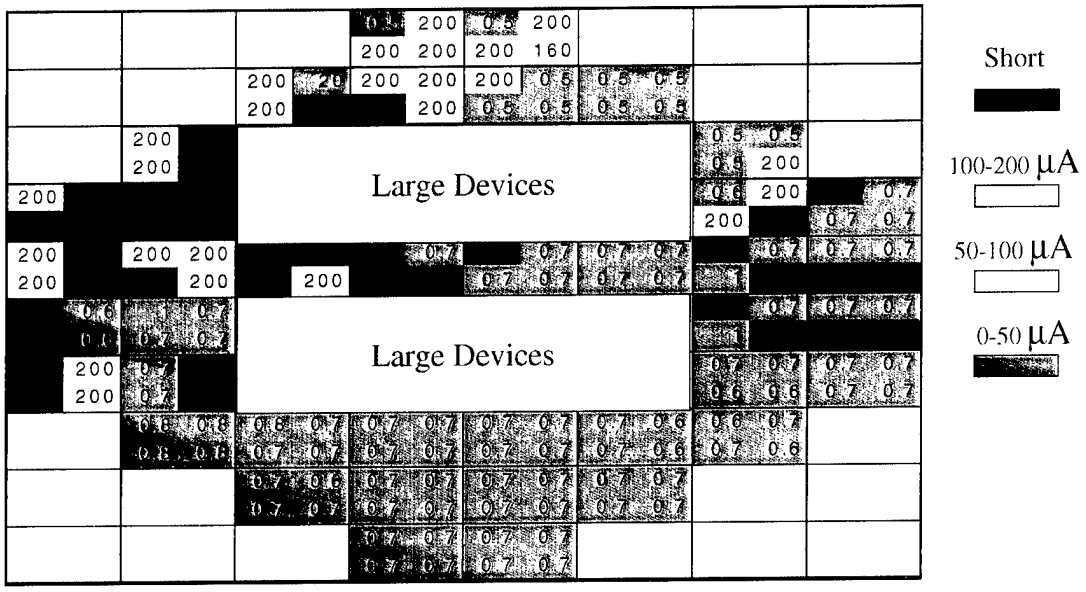


Figure 3-17. Wafer map of leakage current, I_r, measured in μA at V_r=- 6 KV and 25 °C for SiC PiN diodes with junction area of $6.4x10^{-3}$ cm^2 and 70 μm epi. Each cell shows the corresponding I_r value in μA.

current, I_r, and forward voltage drop, V_f. As seen in the histogram of Figure 3-15, the BV distribution peaks at 5 KV and decreases with a long tail toward lower voltages. These data were measured at 25 °C on medium size diodes with junction area of $6.4x10^{-3}$ cm^2, which originated from three wafers. Figures 3-16 and 3-17 contain the BV and I_r wafer maps, respectively, for one of these wafers. These highly correlated wafer maps show a high diode yield in the lower right side of the wafer with respect to the reverse voltage characteristics. The high yield area consists of BV > 5 KV and I_r < 0.7 μA. This type of geometrical yield partition with good and bad diodes clustered on different halves of the wafer suggests that starting material quality and physical characteristics caused the yield loss, because process-induced variations usually do not produce these yield contours.

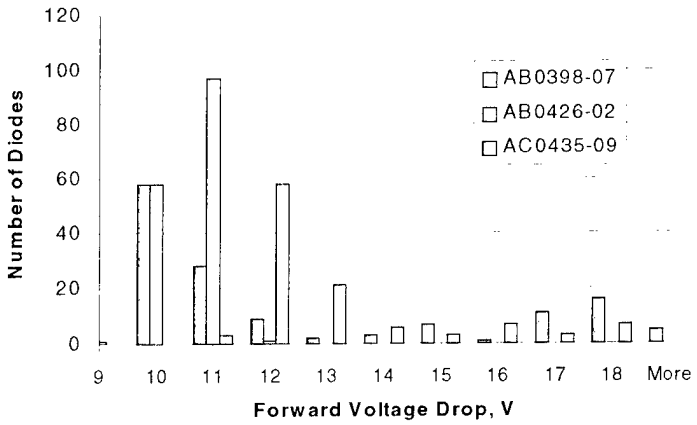


Figure 3-18. Histogram of forward voltage drop measured at 1 A (156 A/cm^2) and 25 °C for SiC PiN diode with junction area of $6.4x10^{-3}$ cm^2 and 70 μm epi.

Figure 3-18 shows the histogram of the forward voltage drop, V_f, for diodes belonging to the same group of wafers. The distribution peaks at V_f = 11 V with no values < 9 V. Instead it forms a very long tail toward higher voltages up to 18 V, except for one wafer with a tight distribution in the range 10 V -12 V. With great surprise we found that the diode yield for an acceptable range of BV, I_r and V_f did not correlate with the grade,

micropipe density and cost of the wafers. The best yield (41%) was obtained with a standard micropipe density, research grade wafer, whose only process difference was a backside nitrogen implant to decrease the backside contact resistance. The other two wafers, that were both production grade with low micropipe density, produced yield figures of 16% and 24%. Although too few wafers were processed for assigning a statistical validation to this unexpected correlation between diode yield and manufacturer-graded wafer quality, this finding need further investigations to achieve production readiness in SiC power technology.

3.1.6. Switching Test Results

In most power electronics applications diode reverse recovery switching losses are a significant part of the overall losses. In addition to direct losses due to diode reverse recovery, this phenomenon causes indirect turn-on losses of the main switching devices, such as IGBTs, MOSFETs, etc. Other adverse effects include EMI and additional thermal management. Unfortunately, silicon diodes have reached their theoretical limits in terms of reverse recovery time. Therefore, there is little hope of reduction of the excessive Si diode reverse recovery time, especially at high blocking voltage or elevated temperature, unless other diode parameters are sacrificed in a trade-off. State of the art silicon devices exhibit reverse recovery times as low as 25ns. Any reduction in reverse recovery time would require a drastic improvement of the current technology or a change from Si to a wide bandgap semiconductor material, such as SiC.

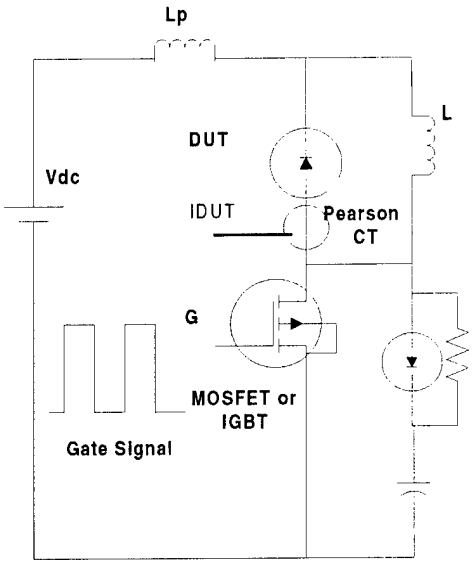


Figure 3-19. Diode reverse recovery test setup

SiC physical properties allow in theory to reduce the diode reverse recovery time and to achieve simultaneously low on-resistance at high blocking voltage with low reverse leakage current. This has been verified with

Table 3-2. Summary of Diode and IGBT Losses due to Diode Reverse Recovery

	Temperature = 25 °C			Temperature = 150 °C		
	Fast Si Diode	**UltraFast Si Diode**	**SiC Diode**	**Fast Si Diode**	**UltraFast Si Diode**	**SiC Diode**
Diode Losses	344 µJ	86 µJ	8 µJ	704 µJ	268 µJ	26 µJ
IGBT Losses	320 µJ	88 µJ	56 µJ	912 µJ	172 µJ	56 µJ

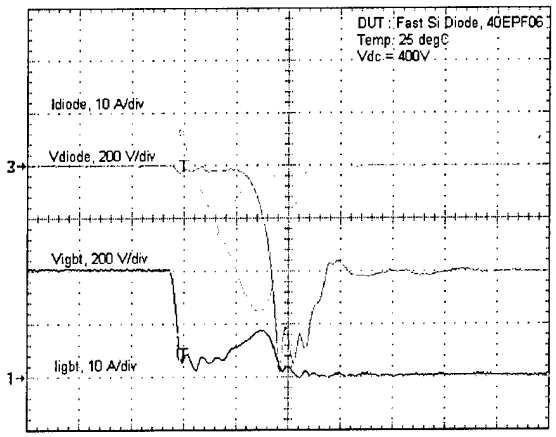


Figure 3-20a. Reverse recovery waveforms for fast diode at 25 °C

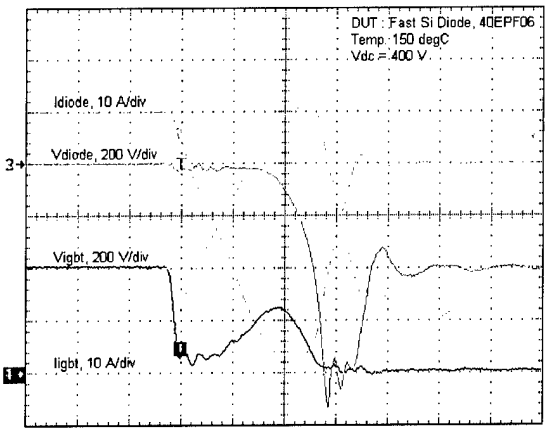


Figure 3-20b. Reverse recovery waveforms for fast diode at 150 °C

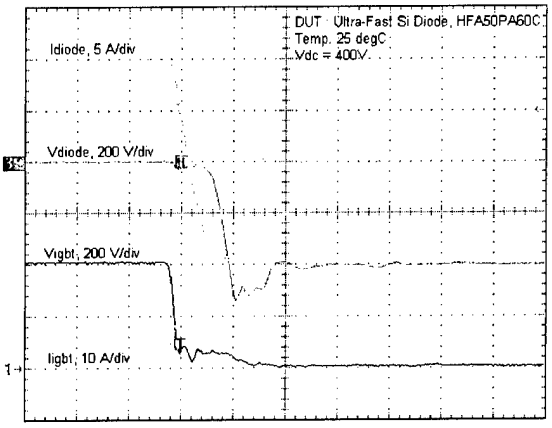


Figure 3-20c. Reverse recovery waveforms for ultra-fast diode at 25 °C

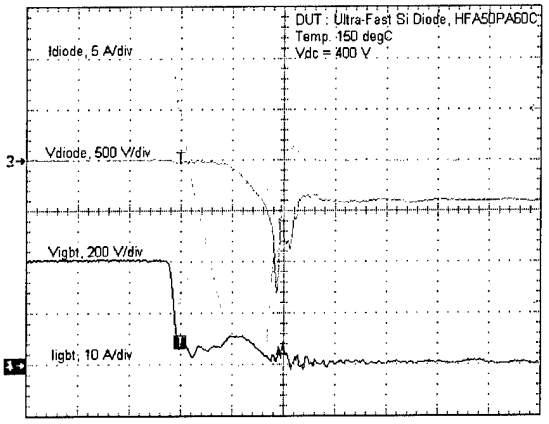


Figure 3-20d. Reverse recovery waveforms for ultra-fast diode at 150 °C

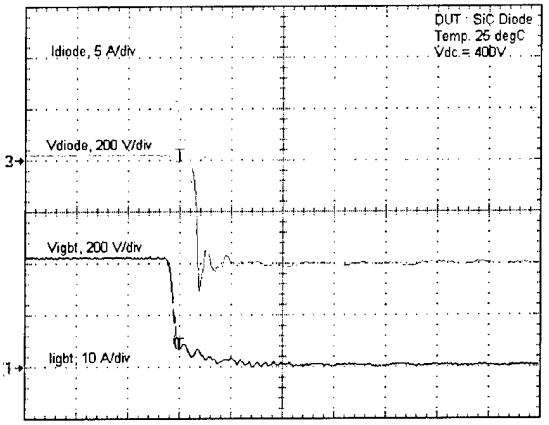


Figure 3-20e. Reverse recovery waveforms for SiC PiN diode at 25 °C

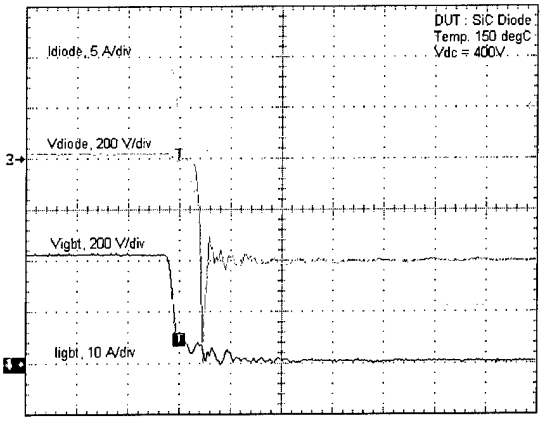


Figure 3-20f. Reverse recovery waveforms for SiC PiN diode at 150 °C

switching measurements on experimental SiC diodes [11]. Proceeding a step further to bring the SiC technology closer to applications, we compared the test circuit effects of SiC diodes built under this program versus fast and ultrafast commercial Si diodes of equivalent rating. We characterized the switching behavior of the test circuit for each type of diode by extracting the reverse recovery time and turn-on losses, not only for the diode, but also for the main switch. The purpose was to demonstrate how the losses of the main switch change as a function of the diode switching properties. Consequently, the overall effect of diode reverse recovery time is magnified in a circuit application. Hence, there is an even greater advantage of using SiC diodes in a hybrid Si/SiC circuit than calculated solely on the basis of diode reverse recovery loss.

Figure 3-19 shows the test circuit used for reverse recovery loss measurement. SiC diodes were tested directly on a probe station. For high temperature measurements the diodes were heated to 150 °C using a thermal chuck. Si diodes were also tested under the same conditions to account for all the circuit parasitics. A fast WARP^{TM} IGBT was used as the main switch. For each type of diode, reverse recovery losses suffered by the diode and the IGBT were separately measured.

Figures 3-20a to3-20f show the switching waveforms of the Si fast, Si ultra-fast and 4H-SiC diodes during reverse recovery at room temperature (25 °C) and high temperature (150 °C). At room temperature, one can see how the reverse recovery time and current of the diode have a tremendous effect on the IGBT turn-on losses. As expected, with a SiC diode 92% and 80% decrease in reverse recovery current are observed compared to fast and ultra fast Si diodes, respectively. The reverse recovery time is reduced by 100ns (88%) and by 53ns (81%) compared to fast and ultra fast Si diodes. The reverse recovery voltage is also reduced by 264V (34%) and by 36V (7%) compared to fast and ultra fast Si diodes. The IGBT turn-on losses due to reverse recovery are reduced by 256µJ (71%) and by 32µJ (24%) compared to fast and ultra fast Si diodes. At 150 °C, there is a slight increase in the reverse recovery current of the SiC diode from 2.2A to 3.5A (60%), but still orders of magnitude smaller than for the fast and ultra fast Si diodes. The SiC diode reverse recovery time increases slightly from 13ns to 16ns. The reverse voltage increases to about 808V from 512V at 25 °C. The Si IGBT turn-on losses when used with the SiC diode are not affected by the temperature increase. These results are summarized in Table 3-2.

These results demonstrate the advantage of using SiC devices in power circuits. In addition to providing low switching losses, low voltage and current stress, SiC devices can operate at much higher temperatures. They also are able to operate at very high voltages and very high switching frequency. The benefits for circuit designers are tremendous, especially for applications that require high voltages, such as X-Ray tubes, high temperature, such as aircraft engines power supplies, and high switching frequency, such as high density converters. SiC diodes can also be used in hybrid applications containing SiC diodes and Si gate-controlled switches. The low switching losses, low reverse recovery current and time will allow power converters to operate at high efficiency and low EMI.

3.2. GTO

Silicon-based Gate Turn-Off (GTO) thyristors have been used for long time as the primary switches for high power circuit applications that do not require high speed. However, as higher blocking voltage and higher frequency are required, Si GTOs encounter many limitations, which originate from the physical properties of silicon. Fortunately, SiC relieves these limitations expanding the GTO capabilities.

The high critical electric field of SiC allows for higher doping of the drift region with significant reduction of the on-state specific resistance for a given blocking voltage. This reduces the static power loss in the GTO and also increases the current density leading to a smaller device area for a given current rating. The smaller SiC carrier lifetime increases by many orders of magnitude the GTO switching speed with a turn-off time reduction from ms in Si to µs in SiC. Even if the Si lifetime could be reduced to the SiC level, this would not help Si GTOs. The reason is that the wide drift region required in Si for high voltage GTOs drastically reduces the base transport coefficient and therefore the junction transistor gain, thereby preventing thyristor action.

Symmetrical [12] and asymmetrical [13 to 17] thyristors and GTOs have been demonstrated in SiC. Although they successfully showed proof of feasibility, these devices focused on the evaluation of special features, but lacked a systematic development procedure and the benefit of the latest SiC technology. To overcome these shortcomings, we directed our efforts toward design and fabrication of a highly manufacturable GTO with 5 layers of epi and ion implanted JTE. We followed a vertically integrated development procedure that can be extended with low effort toward development of future SiC GTO versions. Moreover, by incorporating all the necessary device features, we developed a GTO that can be used as a prototype for initial production.

3.2.1. Design

Our objective in designing the GTO was to optimize the electrical characteristics while adopting a low risk approach, consistent with the current maturity level of SiC technology. The goal was to produce functional devices for the SiC half-bridge inverter according to program requirements. Therefore, we selected an all-epi layer structure using ion implantation only for the JTE edge termination and additional doping of the gate contact region. Contrary to the commonly-used npnp polarity of Si GTOs, we chose N^+ 4H-SiC as starting material to provide a high conductivity substrate and high vertical electron mobility. The main design effort consisted of adjusting the doping concentration and thickness of the various epitaxial layers. Both analytical and numerical analysis were used in 1-D and 2-D modes. The resulting structure is shown in the cross-section of Figure 3-21. Design refinements were made between process iterations using feedback from electrical measurements.

This GTO design consists of five epi layers, of which the two extreme ones form the anode and the cathode. These layers are heavily doped to provide high injection

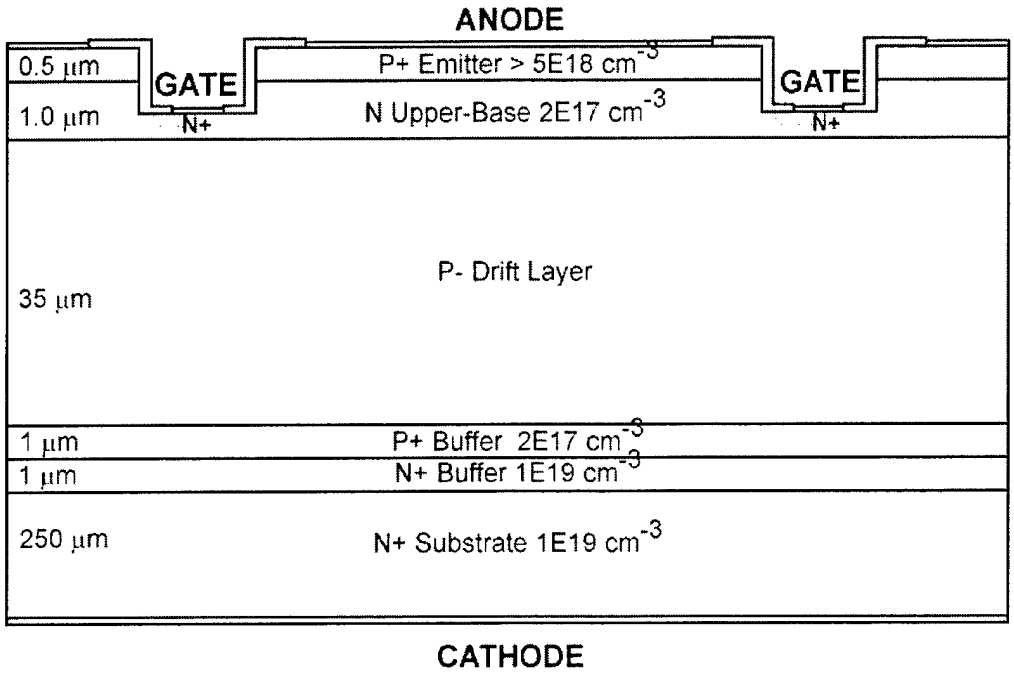


Figure 3-21. GTO cross section.

efficiency while the doping and thickness of the internal layers are chosen to maximize the forward blocking capability and the current gain of the upper pnp transistor. We selected an asymmetric configuration to reduce the thickness of the drift layer and achieve faster switching speed with lower conduction loss than with the symmetric approach. The asymmetric configuration includes a p-type punchthrough buffer (PTB) layer over the cathode to avoid punchthrough breakdown from the p-base to the cathode in the forward blocking mode, that is with positive voltage applied to the anode. The penalty for this extra layer is a reduced reverse breakdown voltage, because the lighter doped side of the cathode junction is formed by the PTB layer instead of the p-base. Another advantage of the asymmetric approach is a reduction of the current gain of the lower npn bipolar transistor which improves the GTO turn-off capability.

The design of the p-type drift layer is mainly determined by the blocking voltage or the available drift layer thickness. In the asymmetric GTO design the portion of the blocking voltage supported by the p-side is spread between the drift layer and the PTB layer. The doping and thickness of this layer must be adjusted to avoid punchthrough of the internal junction space charge layer to the cathode junction under forward blocking conditions. Typically, for a 1 μm thick PTB layer a doping of $2\text{-}4\text{x}10^{17}$ cm^{-3} is appropriate, as shown in Figure 3-21. The PTB layer doping also influences the current gain of the lower npn transistor by affecting the emitter injection efficiency of the cathode.

Similar constraints apply to the design of the n-base. Firstly, the doping concentration and thickness of this layer must be adjusted to support the n-side portion of the blocking voltage without punchthrough to the anode. Secondly, the n-base properties must provide

the required npn transistor gain by determining the emitter efficiency of the anode and the appropriate base transport coefficient. Typical values of the n-base properties are 1-2 μm thickness and 2-4x10^{17} cm^{-3} donor concentration.

Accurate values for all the physical design parameters were derived from 1-D and 2-D modeling , as discussed in section 3.3.2. These simulations also included the effect of the planar dimensions, which are discussed in section 3.3.3. dealing with the GTO layout and test vehicle design.

3.2.2. Modeling

We utilized for GTO modeling the two-dimensional device simulator TMA Medici using a set of experimentally-validated 4H-SiC material parameters. Three different GTO cross sections were investigated. First, a one-dimensional cross-section through the anode allowed to model static GTO thyristor characteristics. Next, a two-dimensional cross section including gate and anode allowed to simulate dynamic switching characteristics. Lastly, a two-dimensional cross section of the device periphery permitted to simulate and optimize the edge termination using a three-zone JTE structure.

Static Characteristics

The thyristor static characteristics were simulated using a 1 x 1 device segment through the anode assuming constant doping in the x- and z-directions. Figures 3-22 and 3-23 show the 1-D simulation mesh and vertical doping profile used in these simulations. For simplicity, the contact resistance to the electrodes and the substrate series resistance were neglected in these simulations.

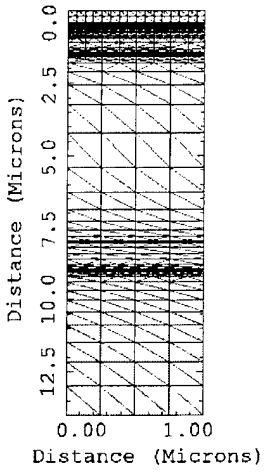


Figure 3-22. Thyristor 1-D simulation mesh.

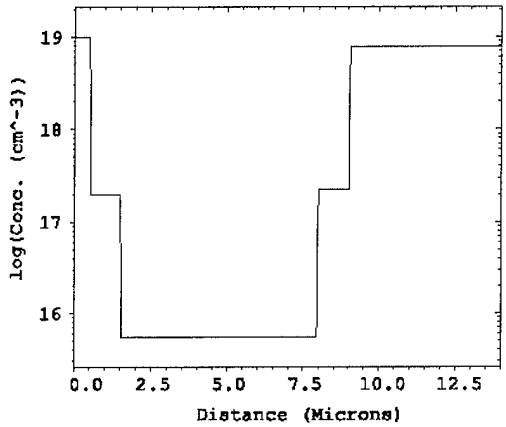


Figure 3-23. GTO doping profile.

Using the above mesh and doping profile, the thyristor was forward biased to obtain the forward blocking and forward on-state characteristics. In this structure, the absence of a gate electrode makes both the upper npn and lower pnp transistors subject to open-base breakdown. In order to make the simulations converge, a temperature of 700K (427 °C) was used to raise the intrinsic carrier concentration and thus avoid numerical noise. As the forward bias increases, the middle junction (J2) remains reverse biased until breakover occurs.

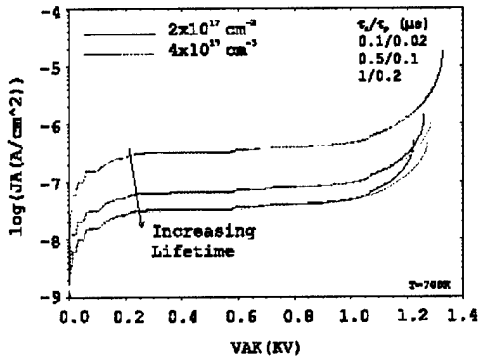


Figure 3-24. Simulated GTO forward blocking characteristics.

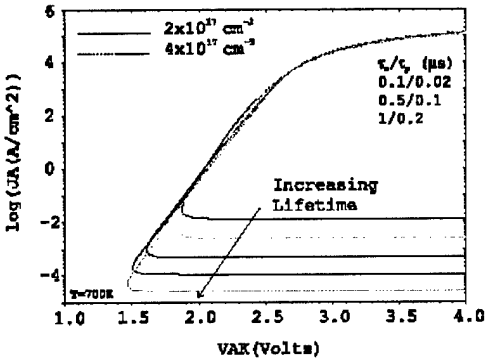


Figure 3-25. Simulated GTO forward on-state characteristics.

Figure 3-24 shows the forward blocking characteristics of the thyristor with n-base doping and carrier lifetime as parameters. The forward breakover voltage ranges from 1220 to 1330 V for the range of parameters investigated. The leakage current decreases with increasing carrier lifetime because of the concomitant decrease of space-charge generation current. Both n-base concentration and carrier lifetime influence the breakover voltage because these parameters affect the upper and lower transistor current gain. As lifetime increases, the transistor current gain increases due to an increase of the base transport factor. This leads to a decrease of breakover voltage by reason of the open-base circuit configuration. The Early effect in the upper base causes the breakover voltage to decrease with lighter n-base doping.

The forward on-state characteristics are simulated by allowing the thyristor to breakover and enter the conducting state. Figure 3-25 shows that the theoretical on-state voltage for these thyristors is approximately 2.3 V at a forward current density of 100 A/cm^2 at 700K. The snapback occurs at different current levels depending on the lifetime and the n-base doping concentration.

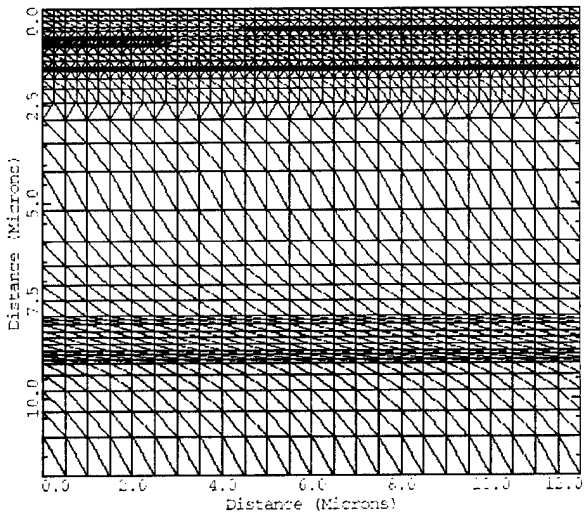


Figure 3-26. Thyristor 2-D simulation mesh.

Switching Characteristics

A two-dimensional mesh is employed to simulate the GTO switching characteristics. The simulation mesh for a thyristor half-cell with anode width (WA) of 15 μm is shown in Figure 3-26. The doping profile through the anode is identical to that used in the static simulations and the carrier lifetime is 0.5 μs for electrons and 0.1 μs for holes. As in the static simulations, the intrinsic device is simulated without accounting for the parasitic resistive components. The

switching simulations are carried out by applying on the gate a negative current pulse for turn-on and a positive current pulse for turn-off.

Simulated turn-on characteristics with an on-state current density of 100 A/cm^2 at the anode are shown in Figures 3-27 and 3-28 for two levels of n-base doping. The cathode current shows a rapid transition to the on-state after a delay time of 0.7 μs and 0.9 μs

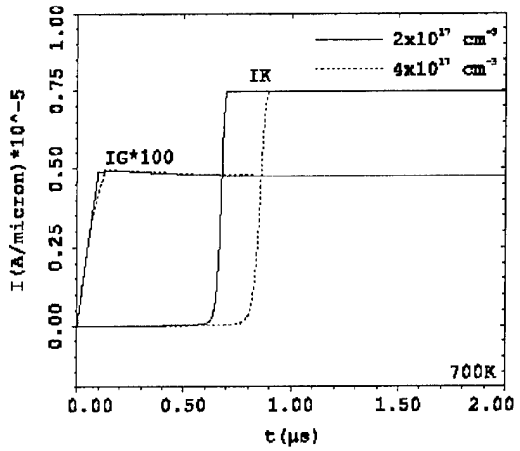


Figure 3-27. GTO current vs time waveforms during turn-on.

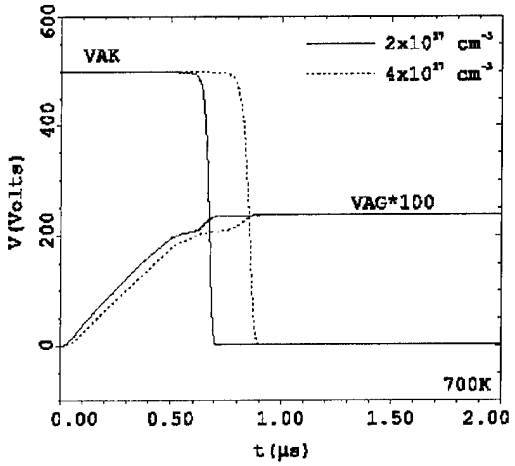


Figure 3-28. GTO voltage vs time waveforms during turn-on.

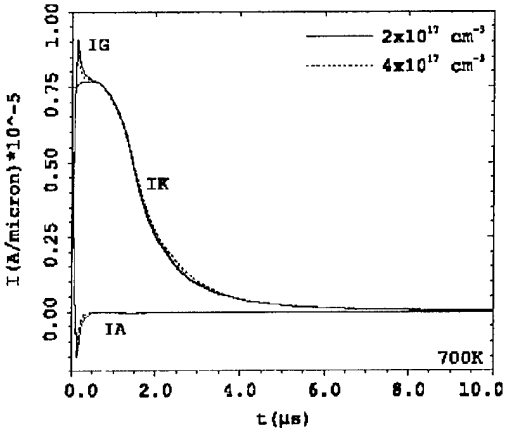


Figure 3-29. GTO current vs time waveforms during turn-off.

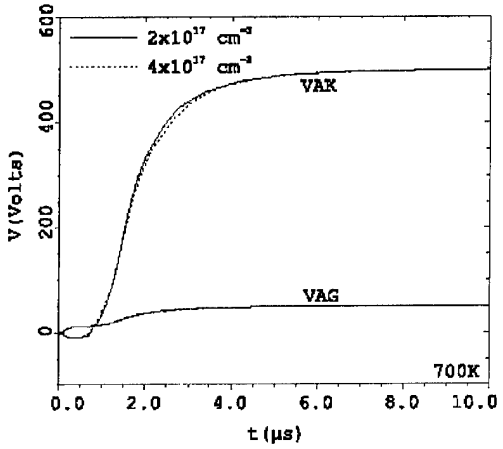


Figure 3-30. GTO voltage vs time waveforms during turn-off.

respectively for n-base doping levels of 2x10^{17} and 4x10^{17} cm^{-3}. The collapse of the anode-cathode voltage shows a similar trend. The longer delay for higher n-base doping results from the increased base transit time due to the wider undepleted base width in the more heavily doped base.

The corresponding simulated turn-off characteristics from an on-state current density of 100 A/cm^2 are shown in Figures 3-29 and 3-30. The turn-off gate current is orders of magnitude larger than the turn-on current. The cathode current reduces to 10 percent of

its on-state value after a delay of 3.2 μs. This delay time was not affected by the n-base doping because turn-off is mainly a function of carrier recombination in the p□ **drift** layer. The cathode current is approximately zero after a delay of 8 μs.

JTE Termination

A three-zone junction termination extension (JTE) scheme has been used for the termination of these 5000 V SiC GTO thyristors. This scheme requires three sequential n-type implants into the p- drift layer and enables the reduction of the surface electric field in a controlled manner according to the width of each zone and the corresponding dose.

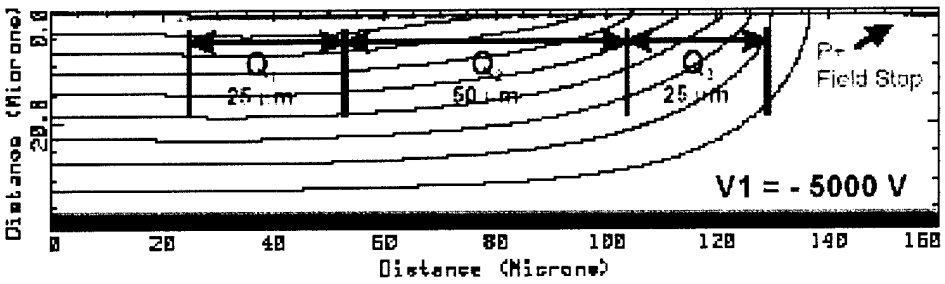


Figure 3-31. Potential lines and doping concentration for 100%, 80%, 60% JTE.

Figure 3-31 shows the termination region of the device used in 2-D modeling to determine the optimum JTE doses. The shaded regions indicate doping concentration and the lines indicate contours of constant potential at a bias of 5000 V between the n-base and the cathode. For the case shown, the three zones are set to 100%, 80% and 60% for the acceptor surface densities, Q1, Q2 and Q3, respectively, where the 100% level corresponds to the critical surface charge density (the product of the critical electric field and the dielectric constant according to Gauss law).
Avalanche breakdown is caused by a buildup of carriers by impact ionization when the electric field approaches the critical electric field. In Figure 3-32 the impact ionization rate is plotted and illustrates that regions of high ionization rate are extended below the

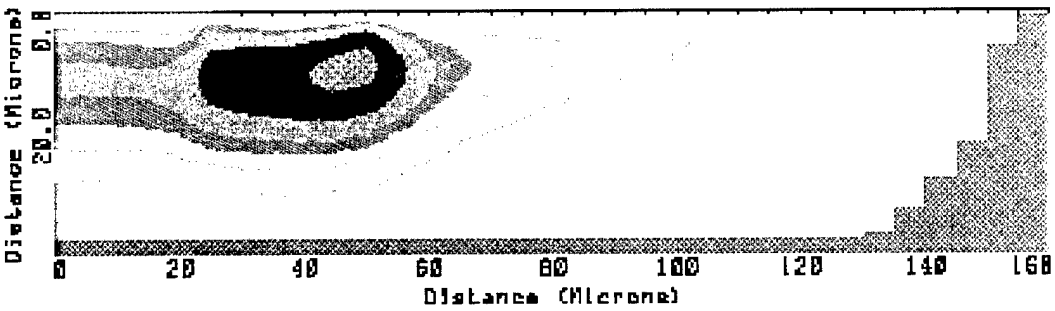


Figure 3-32. Impact ionization rate for 100%, 80%, 60% JTE (BV = 5660 V).

termination region. These contours also demonstrate the effectiveness of the multiple-

zone JTE to gradually spread the field laterally and to remove the high field regions from the surface. Figure 3-33 compares three of the best 3-zone JTE dose schedules and shows that this termination is capable of closely approaching the ideal breakdown voltage of 6000 V for the specified p-epi (35 μm, $1x10^{15}$ cm^{-3}).

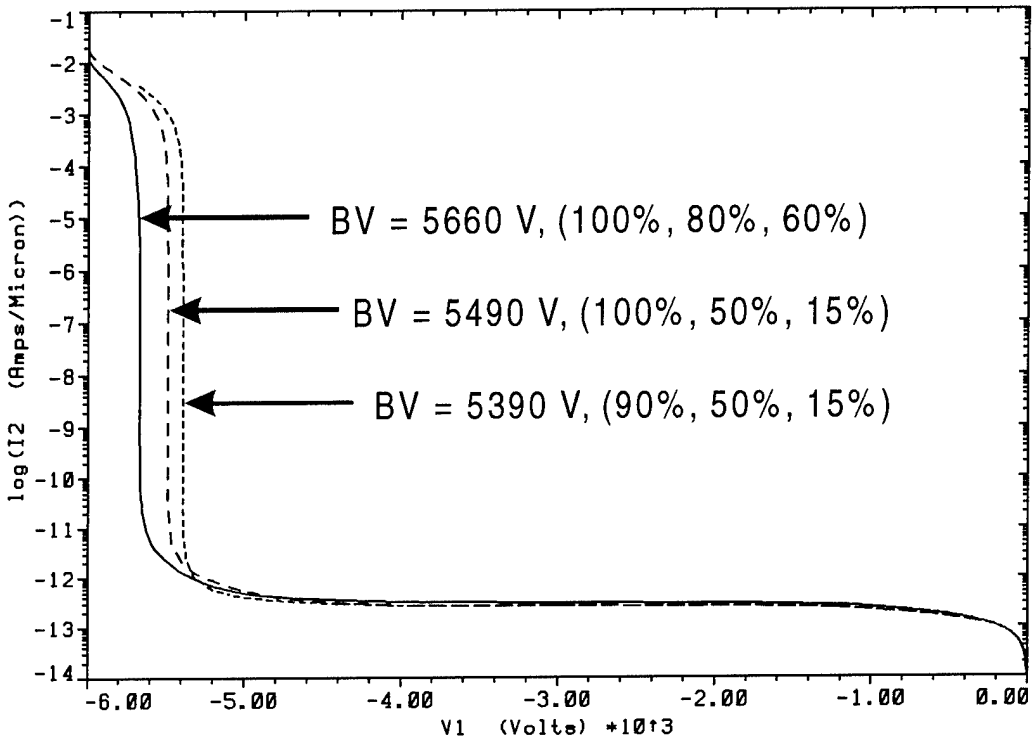


Figure 3-33. Breakdown voltage versus JTE dose schedule.

3.2.3. Layout

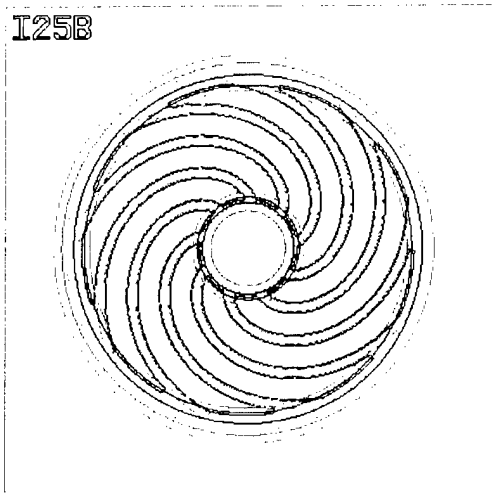


Figure 3-34. Involute GTO layout.

The GTO mask set was designed with several variations in device size and geometry in order to evaluate device yield and performance. A main requirement for GTOs is to minimize current crowding during the initial stage of device turn-on. An additional requirement is that the anode be sectioned into small segments to allow for gate controlled turn-off. These needs are satisfied by an interdigitated geometry, where anode and gate electrode segments are interleaved with each other. Furthermore, to promote even distribution of the conduction current during turn-on or turn-off, these segments must be arranged symmetrically. Three possible geometries comply with these requirements. They are the involute, concentric, and linear patterns. In

this test vehicle, we used involute and concentric patterns of 600 μm diameter and linear patterns of 300 μm x 300 μm and 600 μm x 600 μm sizes.

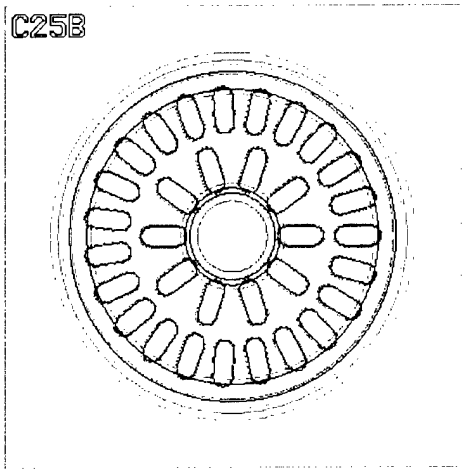


Figure 3-35. Concentric GTO layout.

The involute layout was first applied to thyristors by Storm and St. Clair [18], who found that this configuration improves di/dt capability, making thyristors more tolerant to fast turn-on. The reason for improved turn-on performance is the extremely uniform turn-on over the entire active area due to this geometry. Figure 3-34 shows the involute pattern used on this test vehicle. The involute pattern is unique in that it provides equal distance between the anode and gate at all points along the involute fingers. The main disadvantages are the reduction of active anode area for a given device size and the increase of gate triggering current compared to the conventional thyristor because of the increased gate periphery. Two variations of the involute geometry with different anode width (25 μm and 40 μm) have been incorporated on the mask to investigate their effect on turn-on and turn-off performance.

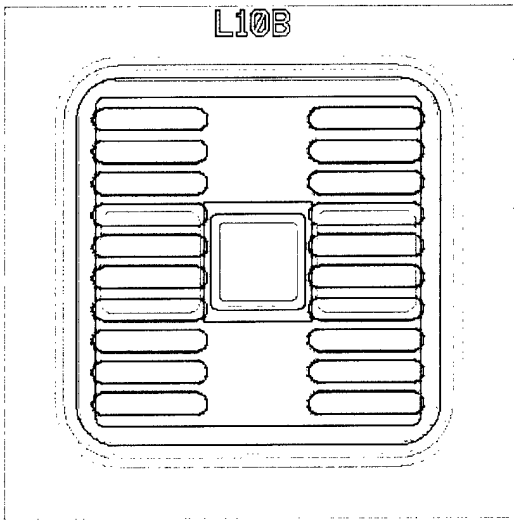


Figure 3-36. Linear GTO layout.

The concentric geometry is the pattern most used in large scale GTOs. Because the whole wafer is used for a single device, the concentric geometry makes optimal use of circular wafers. This geometry is illustrated in Figure 3-35 for a 600 μm x 600 μm device where the anode regions consist of small isolated segments surrounded by the gate electrode. The width and area of these anode segments control the thyristor turn-off performance. A smaller segment width allows control of a larger anode current density and a smaller area allows for faster turn-off time. Three variations in anode segment width (15 μm, 25 μm and 40 μm) have been incorporated in the layout.

The linear geometry is similar to the concentric pattern except that the anode segments are arranged in rows. Both large and small GTO layouts were included to examine size effects. The anode width ranged from 15 μm to 80 μm. Figure 3-36 illustrates the linear layout used in our test mask. In addition to the above GTO designs, a conventional semiconductor controlled rectifier (SCR) was included in this mask set. This design

Table 3-3. GTO layout variations

GTO geometry and Device Size	Test Element	Anode Width W_A (μm)	Anode Length L_A (μm)	Gate Width W_G (μm)
Involute 600 μm Diameter	I25B	25	NA	12
	I40B	40	NA	12
	I25R	25	NA	18
	I40R	40	NA	18
Concentric 600 μm Diameter	C15B	15	60	11
	C25B	25	60	11
	C40B	50	60	11
	C25BS	25	60	11
	C40BS	40	60	11
	C25RU	25	60	15
	C40RU	40	60	15
Linear 600 μm x 600 μm	L04B	83	135	11
	L10B	26	135	11
	L14B	16	135	11
	L04BS	83	135	11
Linear 300 μm x 300 μm	LS02B	79	105	11
	LS04B	34	105	11
	LS06B	19	105	11
	LS02BS	79	105	11
	LS04BS	34	105	11

consists of one continuous anode without the gate interdigitation found in GTO designs. The purpose was to evaluate the GTO characteristics in comparison to conventional SCRs using the same process and starting material.

Table 3-3 summarizes the GTO design variations found in this mask set. The variable parameters are anode width, W_A, anode length, L_A, and gate trench width, W_G. All the devices were designed with the same set of design rules independently of the design variation. In addition, for selected devices, aggressive and relaxed design rules were included to test the effect on yield. To assess the edge termination effectiveness, some devices have both terminated and unterminated versions. Also, emitter shorts were provided on some designs to evaluate their effect on open-base breakdown of the upper pnp transistor. Small versions of the involute and concentric geometries were not possible because the electrode pads would have been too small to probe. Therefore, this comparison was limited to the linear geometry GTOs.

Electrical test structures (TEGs) were incorporated in this test vehicle to provide quantitative assessment of doped layers, junctions, and metal contacts for process and device diagnostics. Specifically, sheet resistance and Hall effect test structures were included for monitoring ion implantation and activation anneals. These test structures allow verification of doping, activation, mobility and depth of implanted and in-situ doped epitaxial layers. These measured parameters and their temperature dependence are

Table 3-4. Electrical test structures in GTO test vehicle

Function	Description
Specific contact resistance	6-Terminal Kelvin contact resistance for n- and p-contacts.
Sheet resistance	4-Terminal van der Pauw sheet resistance. (p^+ anode, n-base, n^+ implant, p^- **drift)**
N-base sheet resistance versus pn-junction bias	3-Terminal pinch resistor for measuring depleted n-base sheet resistance.
Hall mobility Hall concentration	6-terminal van der Pauw Hall-effect test structure (p^+ anode, n-base, n^+ implant, p^- drift)
PN junctions	4 sizes of anode-gate pn junctions to monitor junction capacitance and leakage current.

also used in conjunction with device simulations. Pinch resistance test structures associated with the n-base allow for comparison of the actual doping profile with the simulated profile. 4-terminal Kelvin contact resistance test structures are used to measure the specific contact resistance of both n- and p-contacts. Table 3-4 summarizes the test structures included in the GTO mask set.

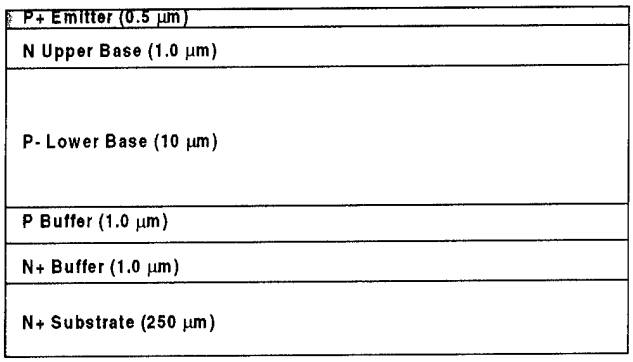
3.2.4. Fabrication

The GTO process sequence is shown in Figure 3-37. The devices were fabricated on 4H-SiC Cree epi wafers with 8° off-axis, 300 μm thick, heavily doped N^+ substrate. Most wafers contained 4 epi layers consisting of a P buffer, P^- blocking region, N base and P^+ anode. Our specifications included an additional buffer N^+ layer over the substrate. However, this was omitted, because wafers with this layer exhibited an intolerably high defect density, which was attributed by the manufacturer to particle deposition during a reactor change between N+ to P+ layers. Hence, the replacement wafers were delivered without the N^+ buffer layer. This contrasts with the composition of the epi wafers used by Cree in their GTO development program [17].

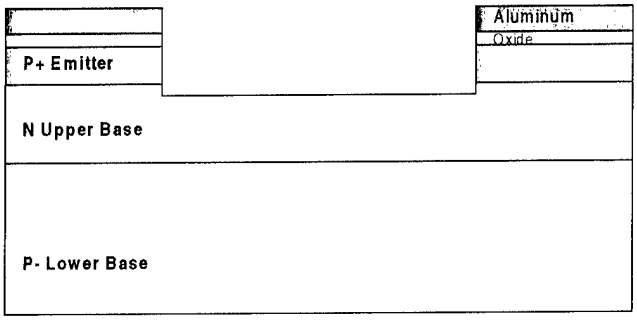
Most of the epi layers are thin and measure 1 to 2 μm, except for the P blocking region, which was 12 μm thick in the first GTO lot and 50 μm in the second. The GTO was designed with asymmetric blocking capability, as determined by the P buffer layer. This layer reduces the non-uniformity of the electric field in the drift region and prevents punchthrough breakdown allowing higher blocking capability. The theoretical parallel plane breakdown voltage for the 12 μm drift region is ~ 2200 V and for the 50 μm is much larger than 5000 V. However, open-base breakdown and field crowding at the device edges reduce the actual forward blocking capability of the GTO, despite the positive influence of the JTE implants.

A mesa approach is employed for the formation of the P^+ emitter and N base, which are defined by SiC RIE etching. Since the N base is connected to the gate, a N^+ implant is used to enhance the donor concentration at the gate contact to lower the contact resistance. A three-zone junction termination extension (JTE) and a p^+ field stop provide

the edge termination for these devices. The JTE zones are ion implanted using successive nitrogen implants at 650 °C. All the implants are activated simultaneously at 1650 °C. After depositing a field oxide, separate contact metals are sputtered over the P+ emitter, N base and backside cathode. Nickel is used over the N^+ and Al/Ti over the P^+. Both are patterned using a lift-off process for contact self-alignment. Ti/Mo is sputtered over the contact metal to form low resistance gate and anode fingers. An interlevel oxide isolates the gate metal from the final metal, which also consists of Ti/Mo. A passivation layer completes the structure exposing the pad contacts.

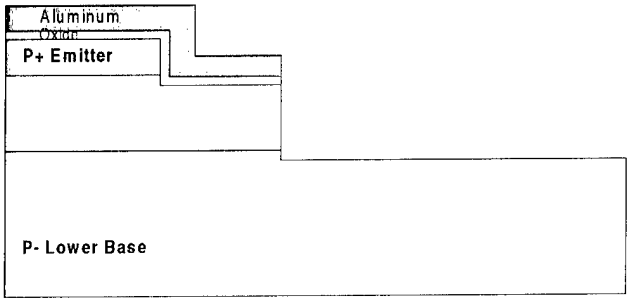


Starting Material
4H-SiC, N+ Substrate
Diameter: 35 mm
P+ Emitter: $1x10^{19}$ cm^{-3}
N Upper Base: $2x10^{17}$ cm^{-3}
P Lower Base: $1x10^{15}$ cm^{-3}
P Buffer: $2x10^{17}$ cm^{-3}
N+ Buffer: $1x10^{19}$ cm^{-3}
N+ Substrate: $1x10^{19}$ cm^{-3}



Etch Trench 1 (for alignment and recessed gate)
Deposit oxide (500 Å)
Sputter Al hard mask (2000 Å)
Pattern **TRENCH1** (Dark Field)
Etch aluminum
Strip resist
RIE oxide (500 Å) and SiC (0.75 μm)

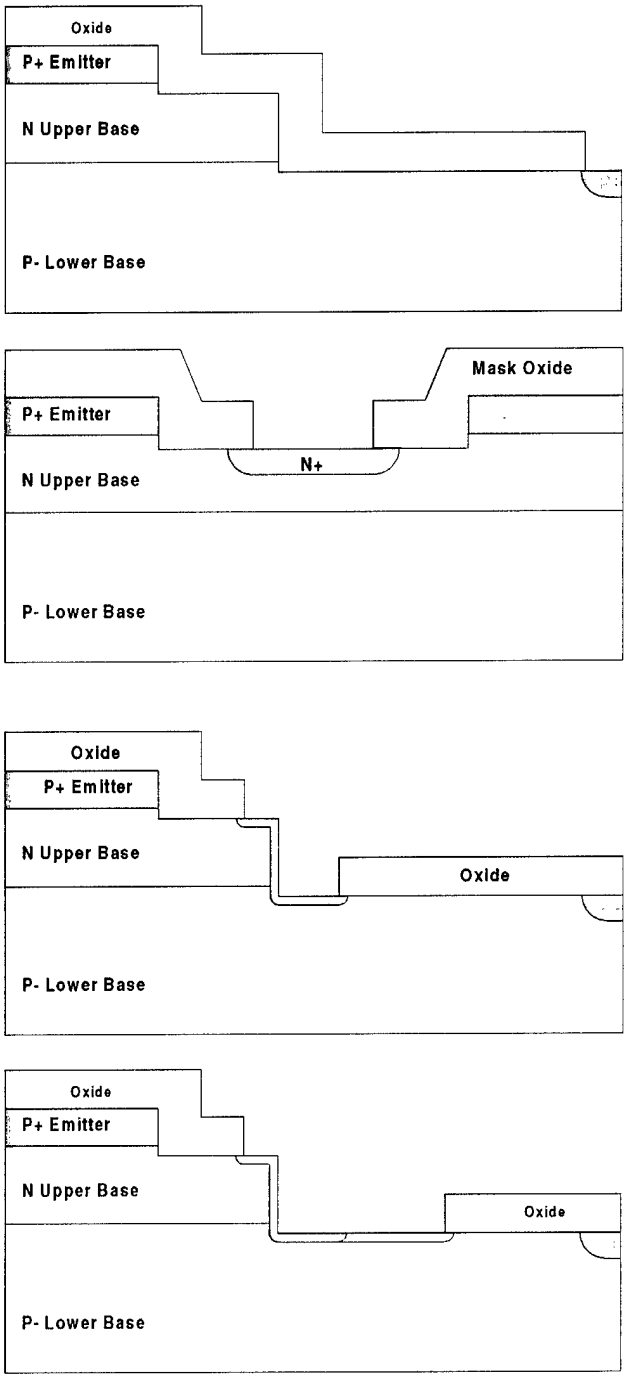
Strip aluminum (2000 Å)
Strip oxide (500 Å)



Etch Trench 2 (for termination)
Deposit oxide (500 Å)
Sputter Al hard mask (2000 Å)
Pattern **TRENCH2** (Dark Field)
Etch aluminum
Strip resist
RIE oxide (500 Å) and SiC (1.0 μm)

Strip aluminum (2000 Å)
Strip oxide (500 Å)

Figure 3-37a. GTO Process sequence



PPLUS Field Stop
Deposit oxide (1 μm)
Densify oxide
Pattern **PPLUS** (Dark Field)
Etch oxide (1 μm)
Strip resist
Deposit screen oxide (500 Å)
Hot Al + C implant

Strip oxide to bare SiC (1.05 μm)

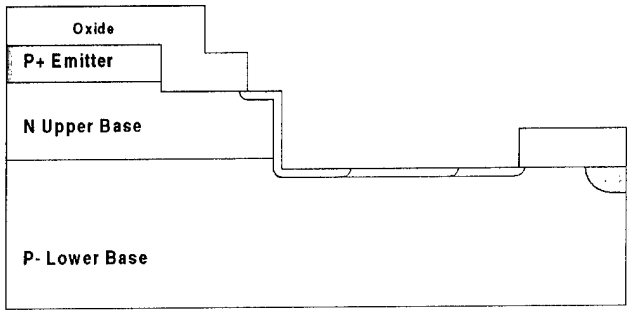
Gate Implant
Deposit oxide (1 μm)
Densify oxide
Pattern **NPLUS** (Dark Field)
Etch oxide (1 μm)
Strip resist
Deposit screen oxide (500 Å)
Hot nitrogen implant

Strip oxide to bare SiC (1.05 μm)

JTE Zone 1
Deposit oxide (1 μm)
Densify oxide
Pattern **JTE1** (Dark Field)
Etch oxide (1 μm)
Strip resist
Deposit screen oxide (500 Å)
Hot nitrogen implant

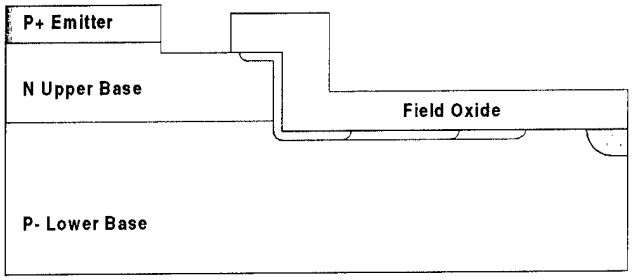
JTE Zone 2
Pattern **JTE2** (Dark Field)
Etch oxide (1 μm)
Strip resist
Deposit screen oxide (500 Å)
Hot nitrogen implant

Figure 3-37b. GTO process sequence.

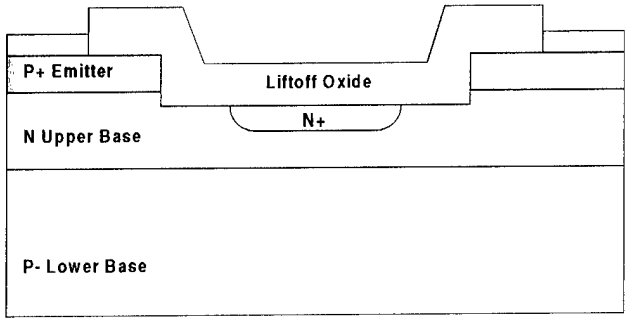


JTE Zone 3
Pattern **JTE3** (Dark Field)
Etch oxide (1 μm)
Strip resist
Deposit screen oxide (500 Å)
Hot nitrogen implant

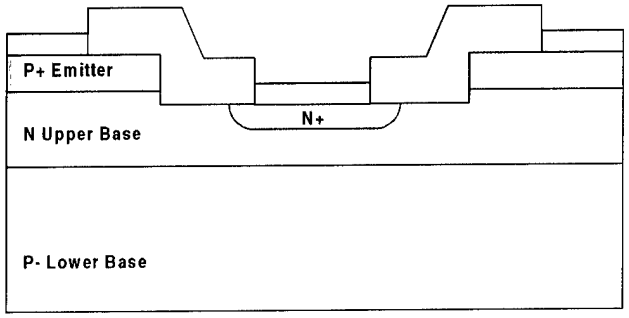
Strip oxide to bare SiC (1.15 μm)
Activate implants



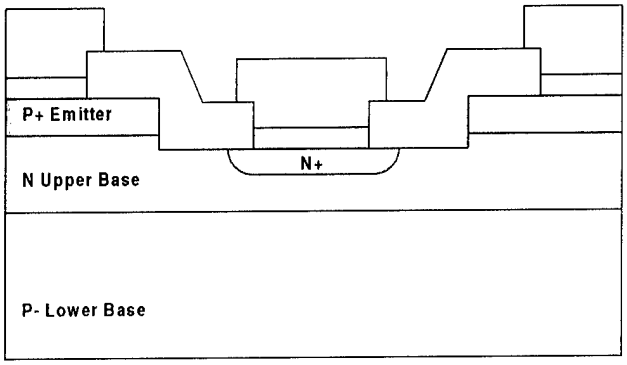
Active
Deposit field oxide (1 μm)
Densify oxide
Pattern **ACTIVE** (Dark Field)
Etch oxide (1 μm)
Strip resist



P-Contact
Deposit liftoff oxide (6000 Å)
Densify oxide
Pattern **PCONTACT** (Dark Field)
Etch oxide (6000 Å)
sputter frontside p-contact
Liftoff p-contact

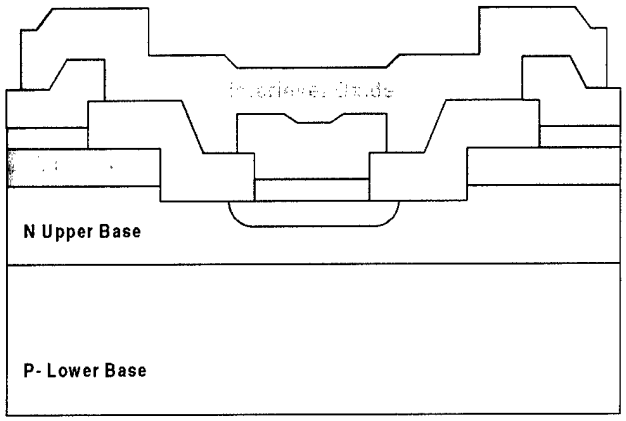


N-Contact
Pattern **NCONTACT** (Dark Field)
Etch oxide (6000 Å)
sputter frontside n-contact
Liftoff n-contact
Sputter backside n-contact
Anneal contacts

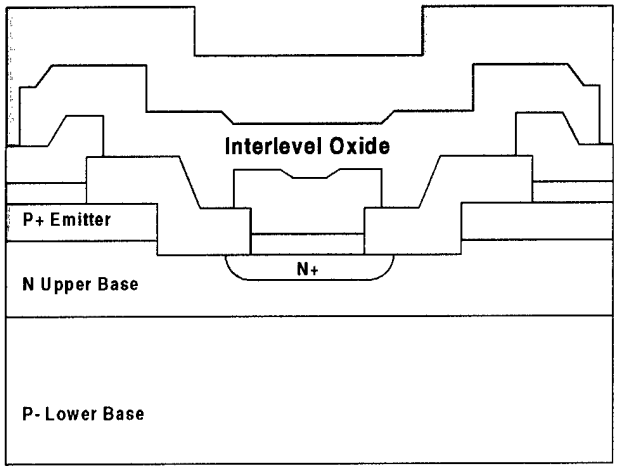


Gate Metal
Sputter Ti/Mo, frontside
Pattern **GATEMETAL** (Dark Field)
RIE Ti/Mo
Strip resist

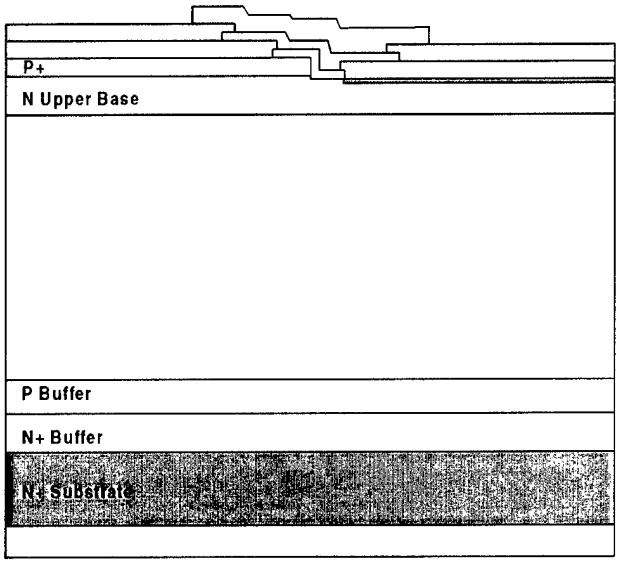
Figure 3-37c. GTO process sequence.



Interlevel Oxide
Deposit interlevel oxide (6000 Å)
Pattern **INTERLEVEL** (Light Field)
Etch oxide (6000 Å)



Final Metal
Sputter Ti/Mo, frontside
Pattern **METAL** (Light Field)
RIE Ti/Mo
Strip resist



Passivation Dielectric
Deposit passivation layer
Pattern **PASS** (Dark Field)
Etch passivation layer

Sputter backside overmetal

Figure 3-37d. GTO process sequence.

3.2.5. RPI Test Results

We investigated the static and dynamic performance of 4H-SiC GTOs made with four epi layers over an N^+ substrate. Although we would have preferred the addition of an N^+ buffer layer over the substrate for a higher quality cathode/p-base junction, this was omitted following the manufacturer recommendation. The reason was the occurrence of a high defect density, which was attributed to the epitaxial growth of this layer in a multilayer structure with many polarity changes. These GTOs were fabricated at GECRD in two lots using Cree wafers with 12 μm and 50 μm thick P^- blocking layer. The corresponding forward blocking voltage was as high as 1100 V and 2900 V, respectively. The on-state static test results are summarized in Table 3-5 for GTOs with anode width of 80μm and cathode area of $5.6x10^{-3}$ cm^2.

Table 3-5. GTO on-state results.

T (°C)	V_{on} (V) @ 10 A/cm^2	V_{on} (V) @ 100 A/cm^2	V_{on} (V) @ 500 A/cm^2	R_{on} (mΩ-cm^2)
25	4.16	5.98	7.89	2.85
50	4.00	5.62	7.69	2.93
100	3.77	5.32	7.40	2.90
200	3.39	4.85	6.72	2.47
300	3.05	4.41	6.29	2.53

Table 3-6 draws a comparison of these results with published data that show the SiC GTO progress in the last 5 years.

Table 3-6. Recent GTO progress.

SiC polytype	P- epi layer thickness (μm)	Forward blocking voltage (V)	Forward voltage drop (V)	Research organization	Year
4H	50	3100	4.97	Cree	2001
4H	50	2900	4.0-6.0	GE/RPI	2000
4H	12	1100	5.7	GE/RPI	1999
4H	7	800	4.0	Rutgers	1999
4H	6	700	4.7	Northrop-Grumman	1997
4H	4.5	400	4.0	Ioffe/Cree	1997
6H	6	90	2.9	Rutgers	1996

These results show a positive progress trend, which stems from higher quality starting material, thicker blocking epitaxial layer, and better device design and processing.

Our GTOs performed better at higher temperature. A lack of latching behavior at room temperature has been attributed to incomplete ionization of the p^+ anode and use of 10^{19}

cm^{-3} doping instead of 10^{20} cm^{-3}, as done by Cree [17]. The transistor current gains of these GTOs were measured as a function of current and temperature. The fabricated devices showed large turn-on gain and small turn-off gain, which are consistent with the respective values of the npn and pnp transistor current gains. These gains were measured using a gate driver circuit, which allows to investigate the switching performance of these GTOs and to analyze separately the npn and pnp current gain of the constituent bipolar transistors.

Although our test vehicle contained three device sizes, i.e. 800 μm, 1200 μm, and 2400 μm, the electrical performance has been characterized mainly on 800 μm devices while the larger devices provided information on device scaling and yield. The measured forward characteristics of an 800 μm device are shown in Figure [3-38] at 150 ºC and 200 ºC. The simulated on-state voltage drop for these GTO thyristors at 100 A/cm^2 and 200 ºC is 2.9 V assuming an ambipolar lifetime of 0.12 μs. For an accurate comparison of measurements and simulations, the parasitic resistance must also be included in the simulations.

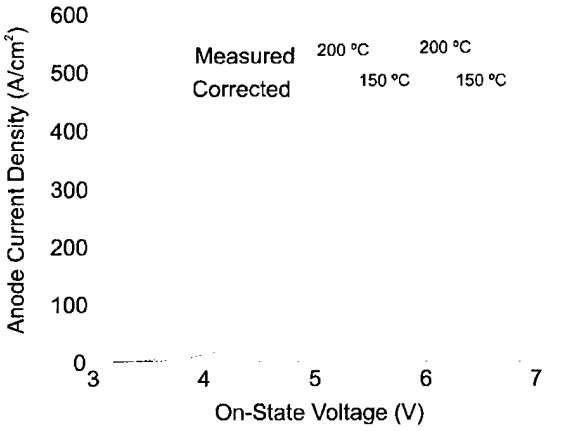


Figure 3-38. On-state characteristics of a concentric GTO; anode area: 4.58x10^{-4} cm^2.

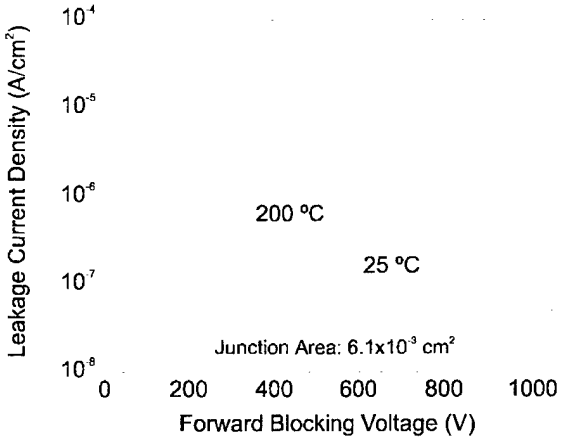


Figure 3-39. Forward blocking characteristics of a concentric GTO; anode area: 4.58x10^{-4} cm^2.

The I-V characteristics after subtracting the voltage drop due to the parasitic resistance are also shown in Figure [3-38]. The corrected forward voltage drop at 100 A/cm^2 is 4.80 V at 150 ºC and 4.55 V at 200 ºC. There is an additional 1.5 V - 2 V drop that is not accounted for by the parasitic resistance and may be caused by poor injection efficiency of the p+ anode or low conductivity modulation of the drift layer. In addition to the large on-state voltage drop, this GTO cannot be turned on at temperatures below 150ºC indicating that the triggering current is very large at low temperatures. At higher temperatures, both the carrier lifetime and the ionization of the p^+ anode increase allowing the device to turn on at moderate current levels (anode-gate current density ~ 2.5 A/cm^2).

The forward blocking characteristics of these devices have been measured up to 200 ºC

and show leakage currents of ~ 10^{-6} A/cm^2 up to the blocking voltage, as shown in Figure [3-39] for an 800 μm device with a blocking voltage of 1000 V. At 200 ºC, the leakage current increases by a factor of 3 and remains below 10^{-5} A/cm^2 until breakdown, which is two orders of magnitude lower than previously reported [19]. The 800 μm devices show a blocking voltage as high as 1100 V whereas the 1200 μm devices show a maximum blocking voltage of 600 V. Open-base breakdown, edge termination or defects may limit the maximum blocking capability of a GTO. In these thyristors, the current-voltage characteristic under forward blocking conditions do not show snap-back up to 200 ºC indicating that the breakdown voltage is limited either by the edge termination or defects.

To characterize device yield, the blocking voltage of the anode-gate junction has been measured for the 800 μm and 1200 μm devices. This blocking voltage must be sufficiently large to allow device turn-off under gate control. For a random sample of 50 devices of each size, the smaller devices show significantly higher yield compared to the larger devices. If devices with anode-gate blocking voltage above 10 V are considered as working devices, the yield for the 800 μm devices is 65 percent while the yield is only 19 percent for the 1200 μm devices. The lower yield of the larger devices is consistent with the larger number of defects present over the larger area.

The GTO switching characteristics have been measured and are shown in Figures [3-40] and [3-41]. These figures show the resistive turn-on and turn-off characteristics of an 800 μm involute GTO thyristor at 190 ºC with an anode finger width of 20 μm. The characteristics are for an anode-cathode voltage of 80 V and an anode current density of 95 A/cm^2. The turn-on characteristics of Figure [3.3-20] show a delay time of 0.8 μs, a

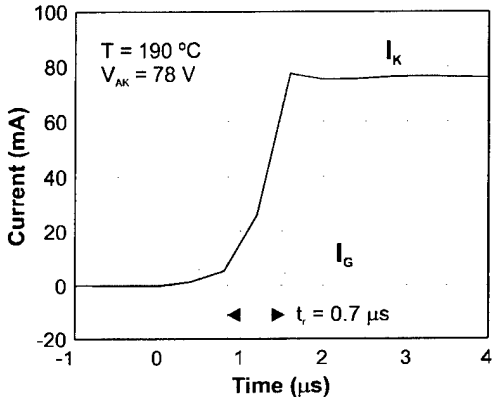


Figure 3-40. Measured turn-on characteristic of an involute GTO at 190 ºC; anode area: 8.2x10^{-4} cm^2.

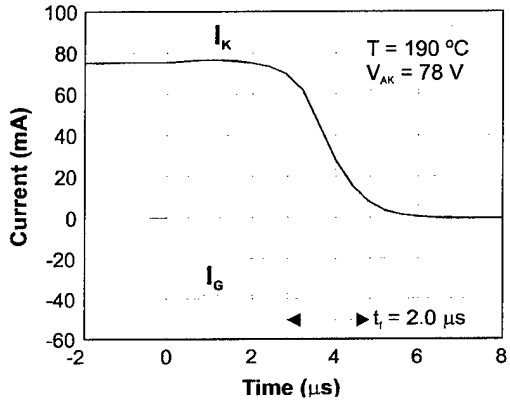


Figure 3-41. Measured turn-off characteristic of an involute GTO at 190 ºC; anode area: 8.2x10^{-4} cm^2.

rise-time of 0.7 μs, and a turn-on gain of 17. For this device, there is no indication of a current spreading phase, which is consistent with the small anode finger width. The turn-off characteristics of Figure [3-41] show a storage-phase of 2.8 μs and a fall-time of 2.0 μs. The recombination tail for this device is less than 1 μs and a turn-off gain of 2 is

measured. A low current gain of the upper pnp transistor may contribute to the low turn-off gain.

GTO thyristor operation is dependent on the behavior of its constituent bipolar junction transistors. In particular, the common-base current gain of each transistor impacts GTO thyristor performance in the areas of holding current, blocking voltage, and switching behavior. Our analysis of the individual transistor gains have explained the measured behavior of these GTOs. The need of high temperature to turn-on these devices is due to the poor performance of the upper pnp transistor, which improves with thermal ionization of the deep p^+ acceptors and consequently leads to higher carrier injection. The low turn-off gain is explained by the similar current gains of both npn and pnp transistors in these GTOs, while for optimal performance the gain of the upper pnp transistor should be large and the gain of the lower npn transistor should be small. A revision of the GTO structure, as defined by the epi thickness and doping concentration, should avoid these problems in the future.

3.2.6. GECRD Test Results

Static and switching measurements were performed at GECRD to complement those done at RPI. These organizations had different motivation. While RPI's objective was a better understanding of the device physics to improve the device design and fabrication, GECRD was interested in characterizing the SiC GTO circuit performance for use in various applications. Consequently, GECRD test results include the determination of the current/voltage ratings and the characterization of the switching behavior.

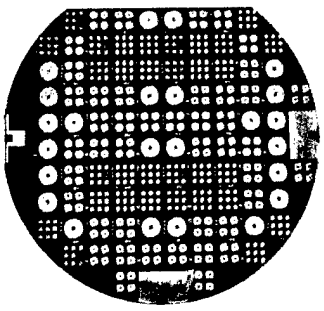


Figure 3-42. GTO test vehicle layout on a wafer.

Figure 3-42 shows the layout of the SiC GTO test vehicle on a 2" diameter wafer. The GTOs are grouped in test element arrays according to size, i.e. one GTO of 2400 μm diameter, four of 1200 μm, and 9 of 800 μm. Figure 3-43 shows the test setup used to pulse the GTOs with a single and a double pulse. Double pulse tests are used to test devices at turn-on when a current is already flowing in the freewheeling diode. This test mimics the kind of conditions generally found in PWM converters, where an upper/lower diode transfers its current to the lower/upper GTOs. The GTOs have to carry both the load current and the diode reverse recovery current. To reduce the amount of reverse recovery current in the GTO at turn-on, we opted for a commercial SiC Schottky diode. These diodes, rated 600V, 6A (SDP06S60) and 300V, 10A (SDP10S30), are currently available for low voltage applications.

Figures 3-44 and 3-45 show the static characteristics of the 50 μm epi GTOs at RT and at 150 °C. Note that the breakdown voltage of these devices is > 2.5 KV and that the forward drop at 1A is on the order of 3-5 V. The dynamic tests were performed with an inductive load both at 25 °C and 100 °C. Gate current, cathode current as well as anode to cathode voltage was measured. Since the gate is referenced to the anode, the cathode

current is the same as the load current and the anode current is the sum of the gate and cathode current.

Figures 3-46 and 3-47 show the GTO switching waveforms at RT and 100 °C for a 1200 μm diameter, 12 μm epi, involute-gate unpackaged GTO. The devices are hard driven with a high gate current at turn-on. At turn-off, the gate current is on the order of 680 mA at RT and increases to 920 mA at 150 °C for a load current of 4A. In terms of gain, the SiC GTO gain at turn-off is on the order of 8 (a higher than typical value for Si GTOs) at RT and decreases to 4 (a typical value for Si GTOs) at high temperature. Turn-off time is on the order of 600 ns at RT and increases to 720 ns at 100 °C. These turn-off times are much lower than similar values for silicon devices. Although the present size difference between Si and SiC GTOs compromises this comparison, it is conceivable that SiC GTOs will remain much faster than similar GTOs even at high current ratings, because of the intrinsic properties of SiC.

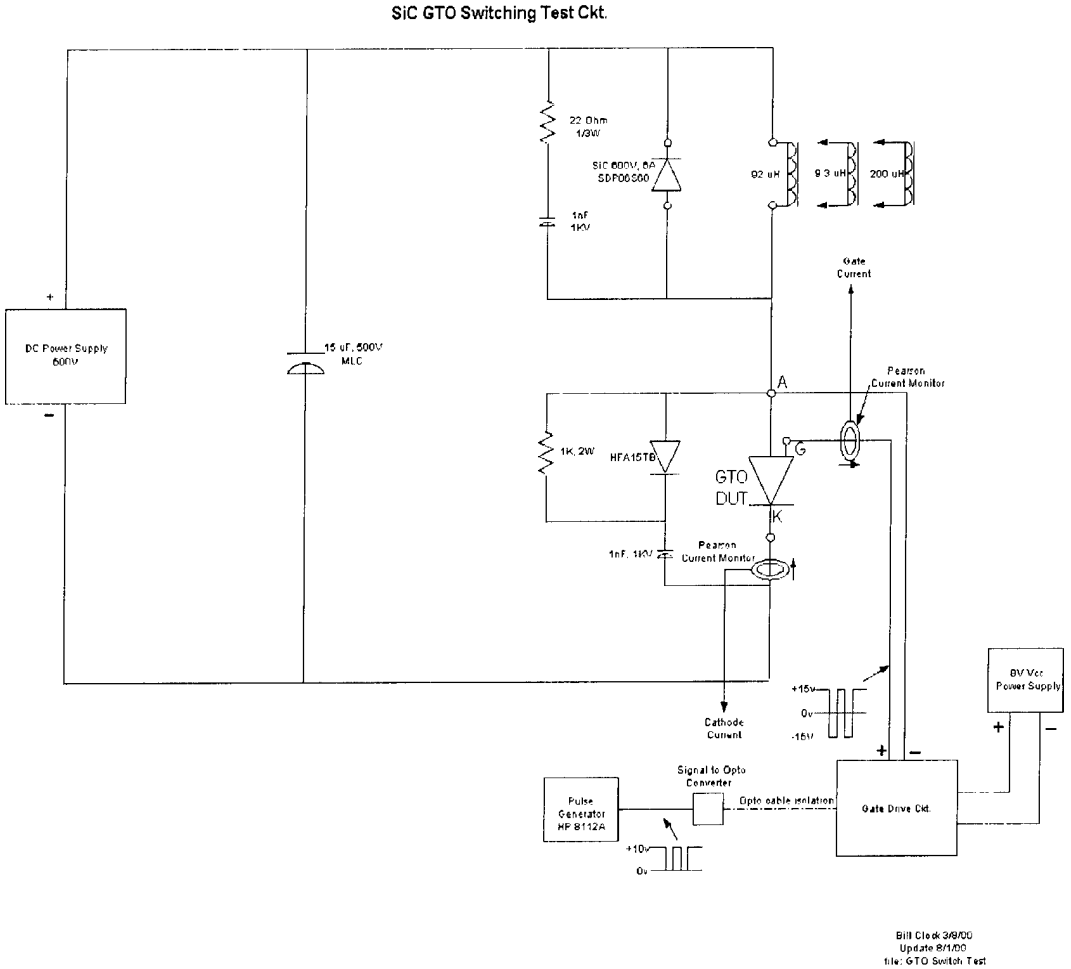


Figure 3-43. SiC GTO test setup.

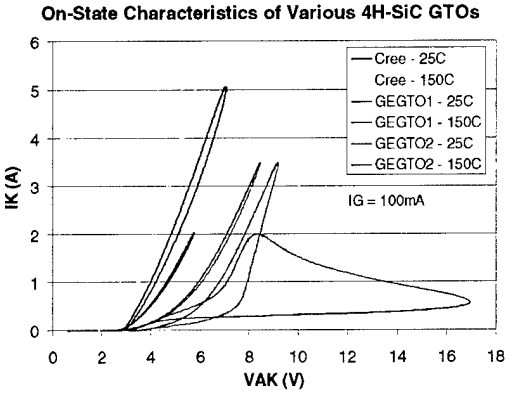


Figure 3-44. SiC GTO On State Characteristics.

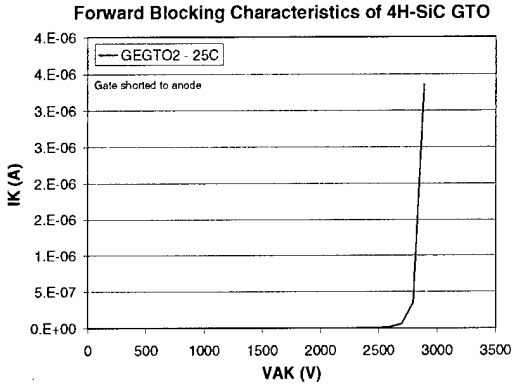


Figure 3-45. SiC GTO Breakdown Voltage.

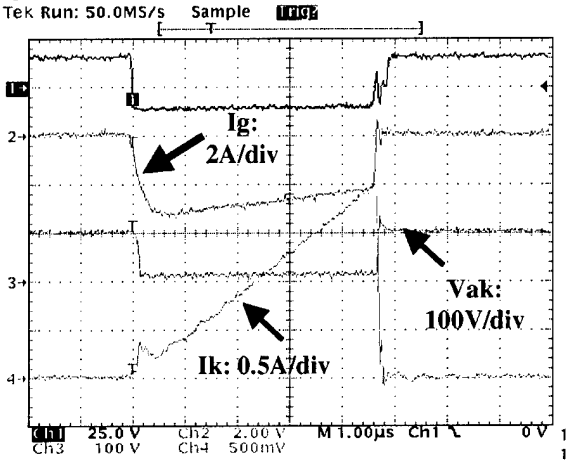


Figure 3-46. Unpackaged SiC GTO Switching waveforms at 25 °C. T_{off} = 600 ns, Ig_{off} = 680 mA.

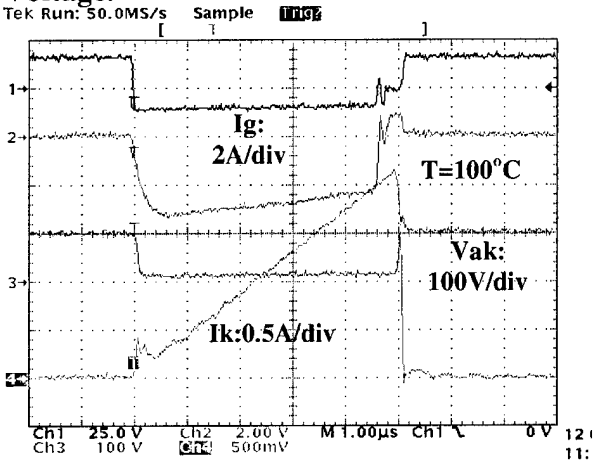


Figure 3-47. Unpackaged SiC GTO Switching waveforms at 100 °C. T_{off} =720 ns, Ig_{off} = 920 mA.

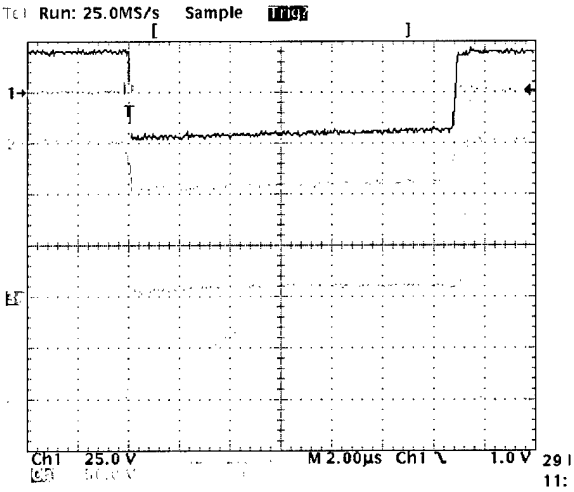


Figure 3-48. Soft-driven packaged SiC GTO switching waveforms.

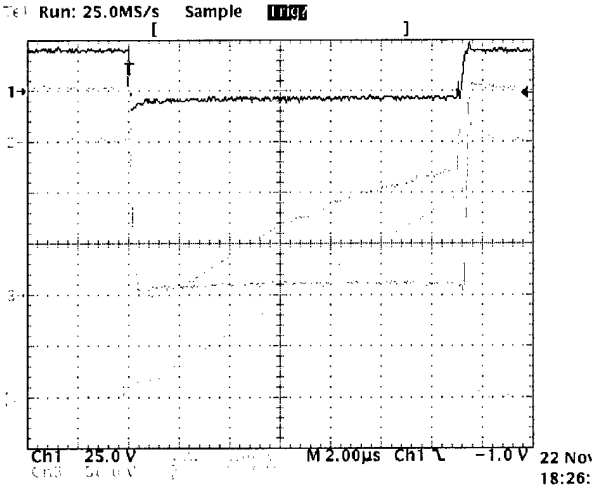


Figure 3-49. Hard-driven packaged SiC GTO switching waveforms.

Figures 3.3-7 and 3.3-8 show 200 V, 4 A switching waveforms of packaged GTOs. In Figure 3.3-7 the devices are soft driven using a resistance in series with the gate. Hence a lower gate current is required to turn the devices on. In Figure 3.3-8 the devices are hard driven and a much higher current is required to turn them on. The gain at turn-off remains the same (on the order of 2). The devices exhibit a very fast turn-on and turn-off.

These results lead us to forecast that SiC GTOs will become viable in the next 3 to 5 years as the material is improving and larger wafer diameters are produced. Although the SiC advantages over Si are well known, the transition to SiC commercial devices will take some time as circuit and system designers learn to use and rely on this technology. Ultimately, circuit designers will recognize the multiple advantages that this technology has to offer and will include SiC diodes and GTOs in their circuit component library [20].

3.3. DIMOS

For switching the GTOs of the half-bridge circuit we need a SiC power MOSFET with a blocking voltage > 100 V. As normal in power devices, a vertical structure was selected to achieve the lowest specific on-resistance. The question remained whether the MOS channel should be perpendicular or parallel to the surface, i.e a UMOS or DIMOS approach, respectively.

In the UMOS approach the channel is formed on the trench sidewall of an npn stack consisting of epitaxial layers. The term UMOS refers to the trench U-shape. Since the channel doping and gate length are defined during epitaxial growth, this approach was preferred in early SiC MOSFETs, because of its simple fabrication process. However, the devices suffered from low channel mobility and high field stress in the gate oxide at the trench corners, which decreased device performance and reliability [21, 22].

In the DIMOS approach the channel is formed along the periphery of a planar gate electrode by shifting the lateral edges of the P-base and N^+ source implants under the gate. The resulting gap between these edges forms the channel. In silicon this gap is easily formed by diffusion of two gate-masked donor and acceptor implants utilizing the different diffusivity of these elements. For this reason the device is called DMOS, i.e. Diffused MOS. In SiC, the diffusivity of donors and acceptors is negligible at practical processing temperatures and therefore diffusion is replaced by implantation to define the position and depth of the P-base and N^+ source regions. Hence, the term DIMOS means Doubly Implanted MOS. Since the channel is formed on an implanted surface, the MOS interface may be negatively affected by lower carrier mobility, higher interface states density and reduced gate oxide dielectric strength, especially at elevated temperature. Moreover, the gate length is more difficult to control in DIMOS than in UMOS because it relies on the precision of two alignment steps unless a self-aligned process is used. The latter is much more difficult to do in SiC than in Si, because the gate electrode cannot withstand the high temperature required for activating the P-base implant (> 1600 °C).

After careful evaluation of the pros and cons of both approaches, we decided in favor of the DIMOS approach, because it appeared more suitable for manufacturing after solving the current problems. Moreover, we could apply our extensive experience on fabrication of planar SiC MOSFETs for signal conditioning. We were also encouraged by reports of new DIMOS developments with good electrical characteristics [23]. Additionally, while the UMOS characteristics depend heavily on the epitaxial layers quality control, the DIMOS characteristics are entirely determined by the device fabricator providing a cleaner interface between wafer supplier and device manufacturer.

3.3.1. Design

Our DIMOS design is based on a conventional planar structure, as shown in Figure 3-50. The N-channel DIMOS is chosen to exploit the higher mobility of electrons than holes in SiC. This choice requires the use of N/N+ epitaxial wafers as starting material and of a P-type implanted base to host the N-channel. A heavily doped substrate is needed to

minimize the vertical resistance. The thickness and doping of the N^- drift region are adjusted for 100 V blocking voltage. Therefore, the N^- epi layer is specified as 3.0 μm thick with a concentration of 2E16 cm^{-3}. The P-base depth and doping level are tailored to avoid punchthrough to the N^+ source and to provide a threshold voltage of few volts. A second P-type implant is used as JTE all around the device to withstand the high field stress on blocking voltage caused by the edge curvature of the P-base region. The nominal channel length is 2.0 μm, but it may vary due to alignment errors during patterning of the N+ source and P-base implants. The gate electrode is made of molybdenum to match GE CRD's standard process for SiC MOSFETs. However, our partner, RPI, prefers N-doped polysilicon for the gate material. The gate oxide thickness is 1000 Å. Although a thinner gate oxide would have lowered the threshold voltage and increased the gain factor, we chose this value to improve the MOS capacitor yield in spite of the high SiC defect level.

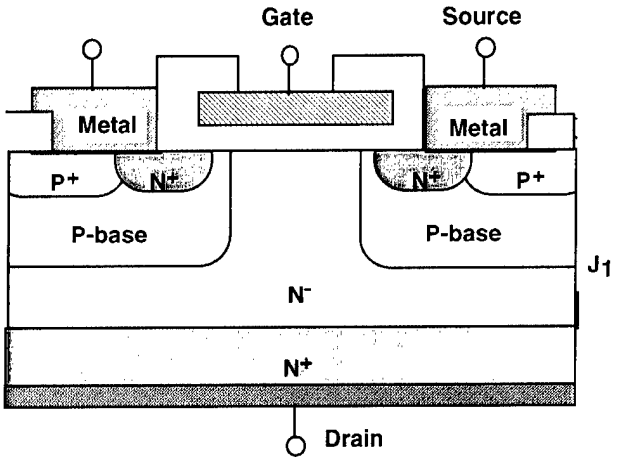


Figure 3-50. DIMOS cross-section

In addition to the above design features there are other ones, for which a definite choice could not be made on the basis of available data. For this reason, we introduced lot splits to mitigate the risk and advance the knowledge base. These splits are shown in Table 3-7.

One split is between 4H- and 6H-SiC. 4H-SiC provides higher vertical mobility, which is beneficial to lower the vertical resistance components in power devices. However, lower electron mobility and reduced gate TDDB (Time Dependent Dielectric Breakdown) have been reported for planar MOSFETs made with this polytype. Since planar DIMOS includes both lateral and vertical conduction, an experimental evaluation is needed to determine the most suitable polytype for this device.

A second split involves the design of the P-base doping profile. Ideally, the P-base concentration should be low near the surface to yield a low threshold voltage and high near the well junction to suppress punchthrough. A retrograde profile will satisfy this need. On the other hand, past experience in SiC has been based nearly exclusively on a multi-energy box profile. However, in this case the box profile should be significantly deeper than the retrograde profile to compensate for the reduced doping level at the well junction, since the entire doping profile is adjusted according to the surface needs. The goal is to maintain a similar acceptor dose per unit area for both profiles to achieve the same punchthrough protection in the P-base. Unfortunately, the extended range of the box profile is beyond the capability of a medium energy implanter, even using doubly ionized charges. An MeV implanter is needed for a boron implant range of 1-2 μm.

During fabrication we found extremely difficult to obtain MeV implant services on SiC wafers at 650 °C and we had to compromise on the range by using conventional implanters.

Table 3-7. DIMOS lot splits

Wafer ID	SiC Poly-Type	P-Base Implant	Implant Anneal Temp.	Implant Anneal Ambient	Anneal Site	Threshold Adjust Implant
Z0358-11 Bottom half (Control)	4H	Retrograde	1600°C	Ar	CRD	No
Z0358-11 Top half	4H	Retrograde	1600°C	Ar	CRD	Yes
U0412-06	4H	Retrograde	1400°C *	Ar	CRD	No
Z0358-09	4H	Retrograde	1600°C	Silane	MSU	No
U0413-08	4H	MeV	1600°C	Ar	CRD	No
L0656-18 Bottom half	6H	Retrograde	1600°C	Ar	CRD	No
L0656-18 Top half	6H	Retrograde	1600°C	Ar	CRD	Yes
L0656-17	6H	Retrograde	1400°C *	Ar	CRD	No
L0656-16	6H	Retrograde	1600°C	Silane	MSU	No
BT0035-16	6H	MeV	1600°C	Ar	CRD	No

* Pbase Implant dose increased to compensate for low activation at 1400°C

The choice of implant activation temperature has been debated during DIMOS design. A low temperature is insufficient for boron activation, which is just few percent under optimal conditions. A high temperature can lead to surface roughness, called "step bunching." DIMOS is particularly sensitive to the surface conditions, because they affect the MOS interface properties. Therefore, a split was introduced to evaluate two possible choices of activation temperature, i.e. 1400 °C and 1600 °C. In an attempt to compensate for the reduced activation at the lower temperature, the P-base implant dose was increased accordingly for the 1400 °C anneal.

While most of the anneals were done in a furnace with a SiC protection in an argon ambient, we also included a split to evaluate the new technique of "silane overpressure," which is thoroughly discussed in the process technology chapter. Our partner, MSU, performed these anneals, but the wafers broke due to high thermal shock in an experimental apparatus. Nevertheless, the experiment demonstrated the ability of this technique to preserve the high quality of the surface finish during temperature anneal above 1600 °C.

A recurrent problem with planar MOSFETs is the occurrence of high threshold voltage. We thought that a nitrogen implant could be used for threshold adjustment, as normally done in Si devices to lower the threshold. For this split we assigned two half wafers, one 4H and the other 6H, to receive a 40 KeV, 1.0E12 cm^{-2} nitrogen implant at 1000 °C,

while masking the other two halves. The dose choice is problematic, because there are no reliable data on the degree of implant activation since it depends on the annealing conditions and interaction with other implants.

3.3.2. Modeling

The selection of the DIMOS device parameters was based on process and device modeling. SUPREM was used to generate the implant schedules for the JTE and P-base implants. MEDICI was used to generate sensitivity curves of key electrical parameters, such as blocking voltage and on-resistance, versus physical and geometrical parameters, such as doping concentration and dimensions of various device regions. These results allowed selecting the wafer specifications, defining the implant and thermal cycles, and guiding the device layout.

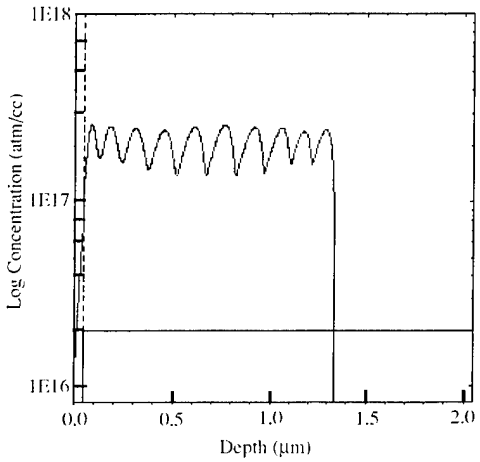


Figure 3-51. P-base doping profile simulation

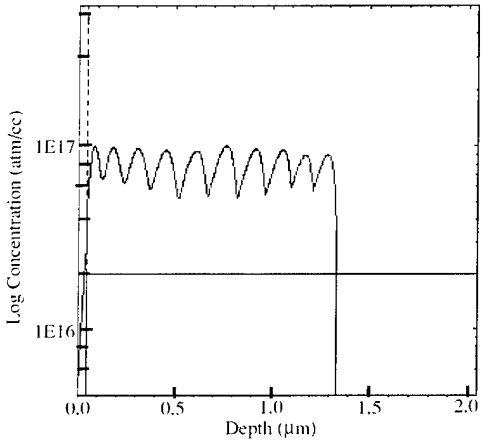


Figure 3-52. JTE doping profile simulation

Figure 3-51 shows the SUPREM simulation of the P-base high-energy implant assuming a box profile. This profile is composed of 10 individual boron implants at progressively higher energy with separately adjusted dose to yield a nearly flat profile with a depth of 1.4 μm. The average concentration is about 1.7×10^{17} atm/cc assuming full activation of all the implanted ions. These depth and doping values were selected from MEDICI simulations. As is well known, only a small fraction of ions are active after annealing. We therefore had to implant a higher dose to compensate for the activation loss. This is a weak point of the modeling effort, because there is little consensus in the literature on the percentage of active boron atoms after annealing. We used a 6% estimate, as reported by Shenoy et al. [23].

Figure 3-52 shows a similar SUPREM simulation of the JTE implant profile. The depth is the same, but the concentration is reduced to about 8×10^{16} atm/cc. This concentration is about 4x larger than the N^- concentration of 2×10^{16} atm/cc, which is marked on the

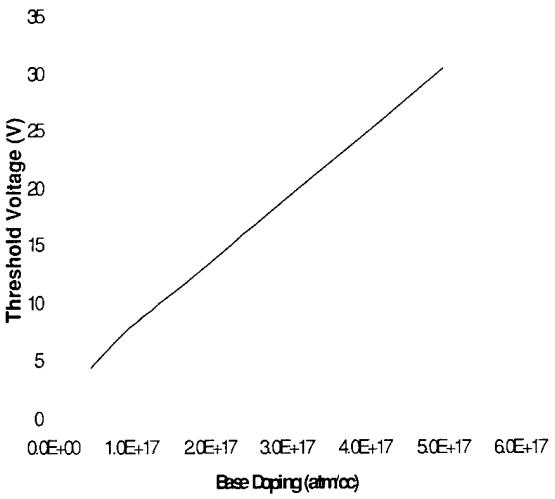


Figure 3-53. Threshold voltage versus P-base doping concentration.

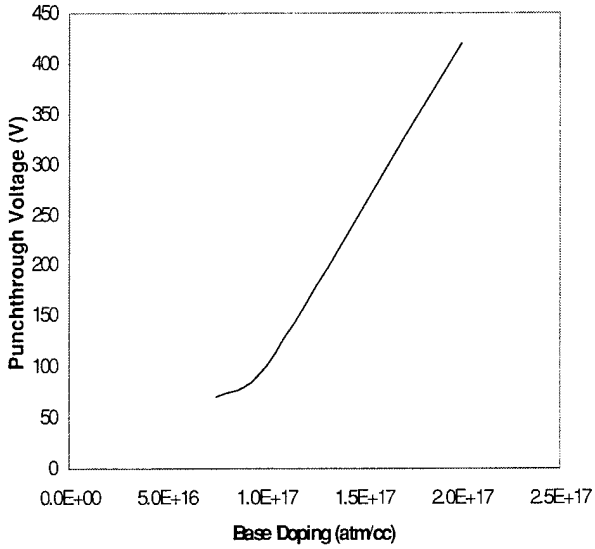


Figure 3-54. Punchthrough voltage versus P-base doping concentration.

graph with a horizontal line. These doping profiles were used for the MEDICI simulations to generate the sensitivity curves discussed below.

A critical requirement for the P-base doping, N_A, is to satisfy the condition that the punchthrough voltage across this region be larger than the blocking voltage specified for this device. Since our DIMOS must withstand at least 100 V in the off-state, a 150 V punchthrough voltage is more than adequate. Hence, from Figure 3.4-5 we can choose a P-base concentration of 1.2E17 atm/cc. The corresponding threshold voltage, V_t, is about 9 V, as extracted from the curve of Figure 3.4-4. This curve shows a nearly straight-line dependence of V_t versus N_A, which differs from the one-dimensional MOS theory. According to this theory V_t should be proportional to the square root of N_A. The discrepancy is attributed to the 2-D numerical modeling performed with MEDICI that takes into account short-channel effects and the geometrical shape of the P-base.

Figure 3-55 shows the calculated dependence of the normalized on-resistance on cell spacing for two channel length values, 1 µm and 5 µm. The cell spacing is the gate electrode width between two adjacent cells. These curves have the characteristic bathtub shape with a wide minimum between 4 µm and 8 µm. The negative slope is caused by an initial reduction of on-resistance with increasing cell spacing, due to widening of the vertical JFET channel under the gate and associated reduction of this resistance component. The positive slope is caused by a reduction of channel length density per unit area with increasing cell spacing. This effect reduces the device area utilization, due to the passive behavior of the gate electrode area in contrast to its periphery, which forms the channel. Therefore, on a normalized basis, the on-resistance increases with increasing cell spacing under these conditions. The concomitant effect of these two actions on the on-resistance results in the relative minimum observed in these curves.

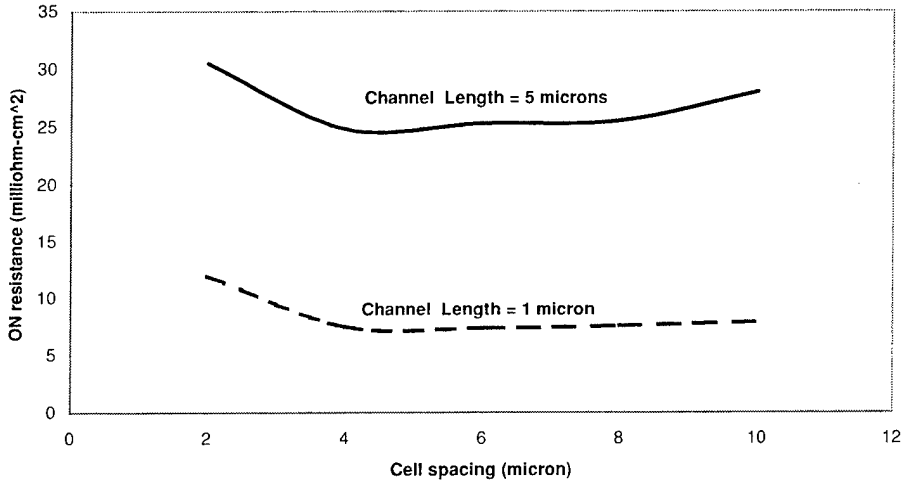


Figure 3-55. On-resistance versus cell spacing for channel lengths of 1 and 5 microns.

A major reduction of on-resistance is achieved by reducing the channel length, where the resistance reduction factor nearly equals the channel length ratio, as seen in Figure 3.4-6. At its minimum, the calculated specific on-resistance for a SiC DIMOS with 1 μm channel length and 6 μm cell spacing is about 7 milliohm-cm^2.

3.3.3. Layout

The main layout features of the 100 V planar DIMOS are as follows:

1. Base-line process and design parameters:
   P-base doping (active acceptors)= 1.2e17 cm^{-3}
   N- drift layer thickness = 3 μm
   N- drift layer doping = 2e16 cm^{-3}
   L_{Gate} (baseline) = 3 μm

2. Masking Layer Assignments:

Step No.	GDS Layer No.	GDS Layer Name	Aligned to Layer	Digitize Data	Purpose
1	1	ALIGN		Clear	Alignment Marks
2	2	JTE	ALIGN	Clear	Define JTE Area
3	4	PBASE	ALIGN	Clear	Define PBASE diffusion
4	5	NPLUS	ALIGN	Clear	Define NPLUS diffusion
5	6	PPLUS	ALIGN	Clear	Define PPLUS diffusion
6	7	ACTIVE	ALIGN	Clear	Define active area
7	8	GATE	ALIGN	Dark	Define polysilicon gate area
8	10	NCONT	GATE	Clear	Define contact window to source

9	9	PCONT	GATE	Clear	Define contact window to PPLUS
10	11	GCONT	GATE	Clear	Define contact window to gate
11	12	METAL	ALIGN	Dark	Define gate and source pad area
12	13	PASS	ALIGN	Clear	Open gate and source pad window

3. DIMOS mask set variations

The DIMOS mask set contains an array of DIMOS devices with various baseline design variations to represent both conservative and aggressive cell dimensions. The variants allow investigating the effect of key layout parameters on the DIMOS characteristics. The cell dimensions are expressed in μm. The DIMOS devices are divided into small and large size, measuring 600μm x 600 μm and 1200μm x 1200 μm, respectively. These sizes were selected to provide an acceptable yield for the current defect density of the starting material. While the small size was chosen to provide statistical yield results, the large size purpose was to demonstrate the present technology capability level.

Small Devices (600μm x 600 μm)

Name of Device	Design	Channel Length (microns)	Cell Spacing (microns)	Contact Metal	Design Rule
BASE3	SQUARE	3	7	Different	Aggressive
BASE5	SQUARE	5	7	Different	Aggressive
JFET3	SQUARE	5	3	Different	Aggressive
JFET5	SQUARE	5	5	Different	Aggressive
JFET9	SQUARE	5	9	Different	Aggressive
RELCH3	SQUARE	3	7	Different	Relaxed
RELCH5	SQUARE	5	7	Different	Relaxed
RELCH10	SQUARE	10	7	Different	Relaxed
SAMESQ	SQUARE	5	7	Same	Relaxed
STRIPE3	STRIPE	3	8	Different	Aggressive
STRIPE5	STRIPE	5	8	Different	Aggressive
STREL10	STRIPE	10	8	Different	Relaxed

Large Devices (1200μm x 1200 μm)

Name of Device	Design	Channel Length (microns)	Cell Spacing (microns)	Contact Metal	Design Rule
BIGBASE3	SQUARE	3	7	Different	Aggressive
BIGBASE5	SQUARE	5	7	Different	Aggressive
BIGREL5	SQUARE	5	7	Different	Relaxed
BIGSTREL5	STRIPE	5	8	Different	Relaxed

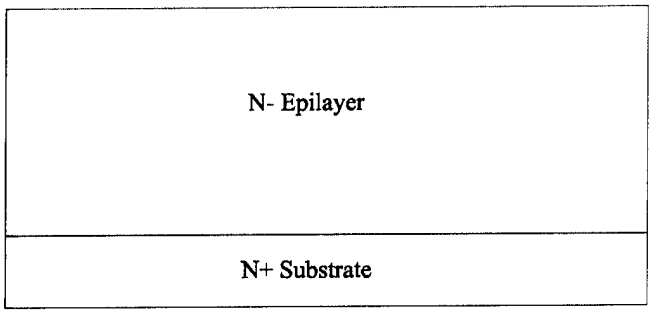
4. Electrical Test Element Group

A test element group (TEG) was included in the mask set for process diagnostic purpose. The TEG elements were designed to measure individual device characteristics, which are integrated in the DIMOS cell. This information permits to analyze the DIMOS performance versus modeling predictions using realistic process control parameters.

1. Van der Pauw sheet resistance structures (Pbase, Nplus, Pplus, JTE, Poly, Nepi)
2. 6-Terminal Kelvin Contact resistance for 4 μm, 6 μm and 8 μm square contacts
3. Linear and Circular TLM for N- and P-contacts
4. Vertical Contacts (dots of different diameters) for N-contacts
5. Hall structures (Pbase, Nplus, Pplus, JTE)
6. P^+/N^- epi diodes of various size
7. P-base/N^- epi diodes of various device size w/o termination
8. N+/P-base/N^- epi BJT (bipolar junction transistor)
9. NMOS and PMOS capacitors
10. NMOS and PMOS gated diodes
11. Short-channel linear NMOS FETs (L_{ch}=1, 2, 3, 5 μm; W_{ch}=50, 100 μm)
12. Short-channel linear PMOS FETs (L_{ch}=3, 5 μm; W_{ch}=50, 100 μm)
13. Linear and Annular MOSFET with long channel
14. Linear MOSFET with long channel length (15, 20, 25, 30 μm) for mobility measurements
15. Short check structures to test shorts between gate and N^+ contacts

3.3.4. Fabrication

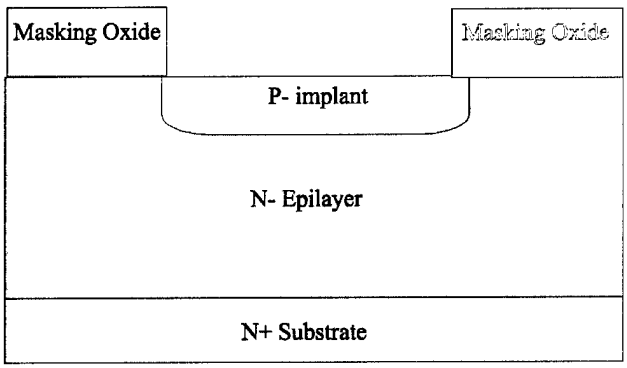
The DIMOS fabrication process is described in Figure 3-56 with device cross-sections at critical process stages accompanied by a corresponding list of processing steps. Unfortunately, only one lot was processed denying the benefit of the test results feedback and preventing the execution of processing revisions. Various technical problems were encountered in MOS processing that required separate short-loop experiments. Shortage of funds and schedule delays forced us to concentrate our efforts on diodes and GTOs eliminating plans for a second DIMOS lot.



Starting Material
N+ Substrate
N- Epilayer :
3 μm; 2e16 cm^{-3}

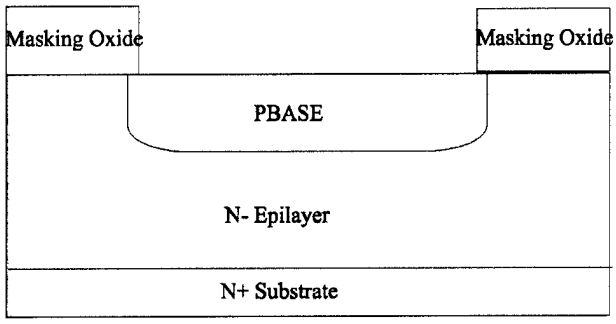
Trench Alignment Key
Pattern ALIGN (mask #1)
Etch ~5000 A^0 Silicon

Figure 3-56a. DIMOS process sequence.



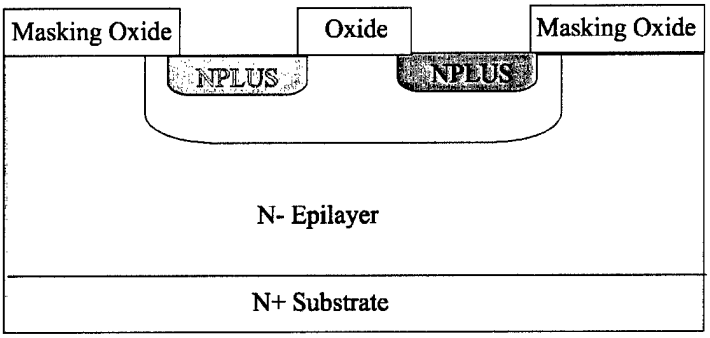
JTE Implant

Deposit oxide for
implant mask
Pattern JTE(mask #2)
Etch oxide
Strip PR
Implant Boron
Strip oxide



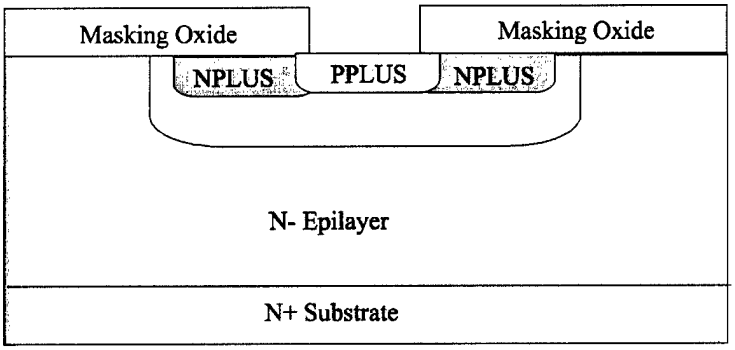
Implant PBASE

Deposit oxide for
implant mask
Pattern PBASE (mask #3)
Etch Oxide
Strip PR
Boron implant :
Xj = 1.0 μm
Npeak = 2e17 cm^{-3}



Implant NPLUS Source

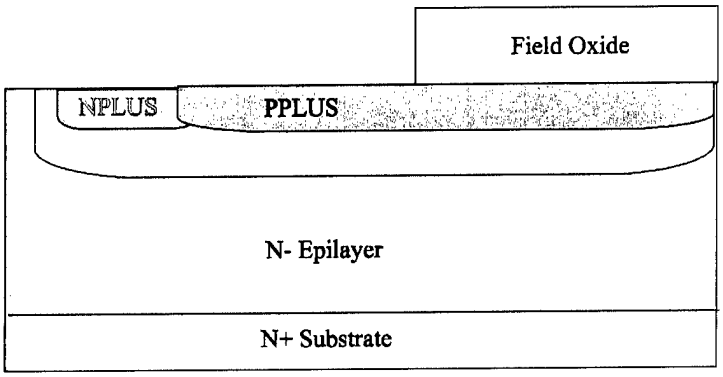
Deposit oxide for
implant mask
Pattern NPLUS (mask #4)
Etch Oxide
Strip PR
Nitrogen implant:
X j= 0.3 μm
Npeak = 1e20cm^{-3}



Implant PPLUS Short

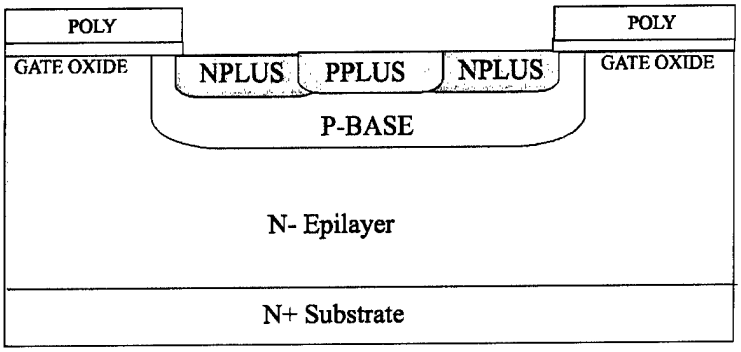
Deposit Oxide for
masking pplus implant
Pattern PPLUS (mask #5)
Etch Oxide
Strip PR
Aluminium implant:
X j= 0.3 μm
Npeak = 1e20cm^{-3}
Strip Oxide to bare SiC
Acitivation Anneal

Figure 3-56b. DIMOS process sequence.



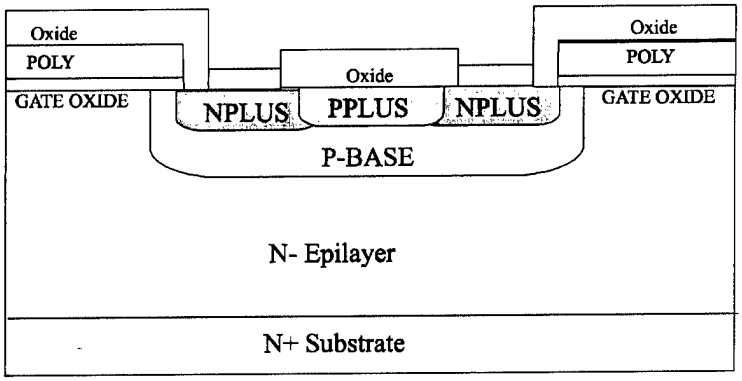
Define Active Area

Deposit Field Oxide
Pattern ACTIVE(mask #6)
Etch Oxide



Gate

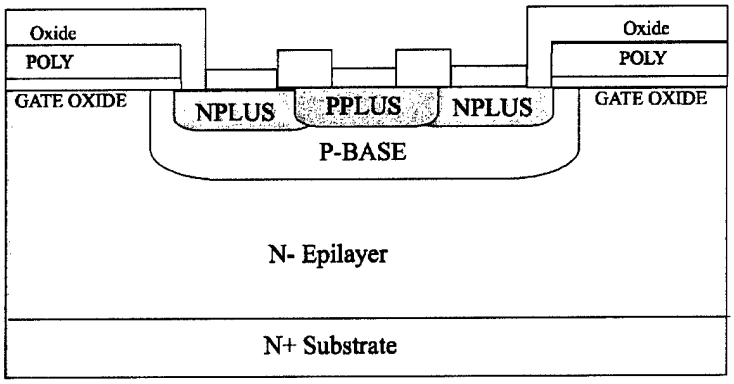
Grow Gate Oxide (~1000 A^0)
Deposit Poly (~6000A^0)
Dope Poly
Pattern GATE (mask #7)
Etch Poly
Etch Oxide
Strip PR



Contact to NPLUS

Deposit Interlevel
Oxide(~6000A^0)
Pattern NCONT(mask #8)
Etch Oxide for lift-off
Deposit Ncontact metal
Lift-off metal

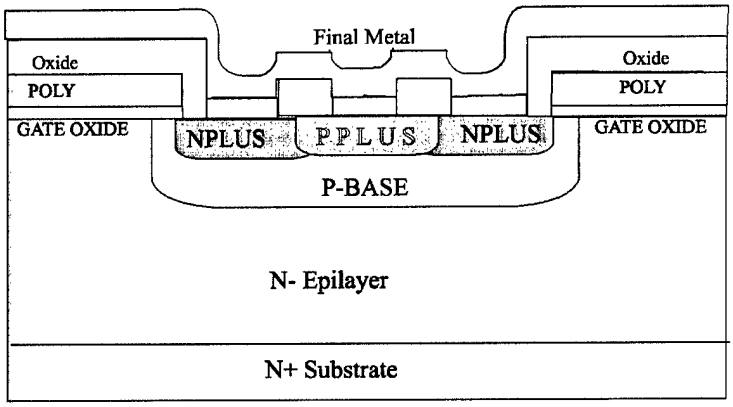
Figure 3-56c. DIMOS process sequence.



Contact to PPLUS
Pattern PCONT (mask #9)
Etch Oxide for lift-off
Deposit Pcontact metal
Lift-off metal

Contact to Gate
Pattern GCONT(mask #10)
Etch field oxide to
expose poly for gate pad

Contact to Drain
Deposit ncontact metal on
back side
Anneal all conatcts



Final Metal

Deposit Final Metal
Pattern METAL(#11)
Etch metal

Figure 3-56d. DIMOS process sequence.

3.3.5. Test results and discussion

The DIMOS lot yielded poor results, since the threshold voltage was in the range of 30-35 V. Therefore, to turn-on the device, it is necessary to apply an electric field of $3x10^6$ V/cm across the 1000 Å thick gate oxide. This field is roughly equal to the dielectric strength of the oxide causing gate breakdown in the weakest devices. The measured threshold is about 6x larger than the predicted value of 6-7 V for the above gate oxide thickness and the nominal p-base doping of $1.5x10^{17}$ atm/cm^3. The discrepancy is attributed to problems with the MOS transistor, characterized by an excessive fixed oxide charge and interface states density.

Despite the little amount of information extracted from this lot, it is possible to suggest appropriate steps for developing future SiC power MOSFETs. First of all, the DIMOS approach appears practical and relatively easy to fabricate. The use of MeV implants for the P-base and JTE is discouraged, because it is difficult to find domestic implant services with this capability. We believe that the retrograde implant can achieve simultaneously high punchthrough voltage across the P-base and low surface doping

concentration in the channel. Moreover, despite a small increment of vertical drift resistance, it is better to start with a lower N^- epi concentration than required by the blocking voltage. The advantage is a decrease of the impurity compensation in the P-base near the surface resulting in a lower threshold. A thinner gate oxide, e.g. 500 Å, is also needed to decrease the threshold, although this choice will not relax the danger of gate oxide breakdown, because this parameter decreases proportionally with oxide thinning.

A normally-off buried channel approach appears superior to the straightforward surface enhancement-type MOSFET used here. This change should minimize the influence of MOS interface charge on the device characteristics and increase the effective channel mobility, as reported by S. Harada et al. [24]. Additionally, the electric field stress in the gate oxide is lower with this approach, thereby increasing the TDDB mean-time-to-failure (MTTF) at high temperature. A buried channel is easily formed using a shallow nitrogen implant. In this program we used a nitrogen threshold control implant in the DIMOS lot, but our dose of $1x10^{12}$ cm^{-2} was too low to invert the polarity of the P-base and we missed the benefits of the buried channel.

The modeling methodology needs improvements as well. Device modeling must comprise more realistic input parameters including MOS interface charge and dopant activation fraction to yield predictions close to the experimental device characteristics. For this to happen, the simulators must be enhanced with additional algorithms and plug-ins for modeling these parasitic effects, which are found in actual devices and processes.

3.4. MOS-Gated Bipolar Transistor

To optimize the electrical performance of power devices a good match must be established between the device structure and the physical properties of the semiconductor. For instance, the Insulated Gate Bipolar Transistor (IGBT) has been a great success for silicon power devices because it combines the high current switching capability of bipolar transistors with the high input resistance and voltage drive of MOSFETs using efficiently the Si material properties.

Unfortunately, IGBTs do not offer the same advantages for SiC. The physical reasons are (1) higher ratio of electron to hole mobility in SiC compared to Si; (2) higher ionization rate of holes than electrons in SiC, which is the opposite of the Si case [25]. Consequently, to obtain an adequate gain factor, an n-channel MOSFET must be selected as the input device. However, with the conventional IGBT structure this choice leads to two undesirable consequences: (1) a high substrate series resistance due to low hole mobility in P-type substrates; (2) a reduced Safe Operating Area (SOA) caused by the high hole ionization rate of *pnp* transistors. Since in an IGBT both the substrate and bipolar transistor types are fixed by the choice of the MOSFET, these drawbacks are intrinsic to SiC IGBTs. An additional disadvantage is the presence of an *npn* parasitic transistor formed by the MOSFET source, P-base and N-drift region, which could cause latch-up in conjunction with the main *pnp* device.

Therefore, for achieving a good SiC power device performance with a similar structure, it is necessary to integrate an N-channel MOSFET and an *npn* bipolar transistor by modifying the conventional IGBT. The result is the MOS-Gated Bipolar Transistor (MGT), which was demonstrated some time ago in Si [26]. Since the MGT contains only an *npn* bipolar transistor formed by the MOSFET source, P-base and N-drift region, a P^+ substrate is no longer needed due to the elimination of the *pnp* transistor used in IGBTs. The danger of latch-up is also removed because there is only one bipolar transistor per cell. As expected, the MGT has demonstrated with numerical simulations good on-state and reverse blocking characteristics with wider FBSOA and RBSOA on account of improved reverse I-V characteristics of SiC *npn* transistors.

An MGT weak point is a larger cell size than that of an IGBT, because of the inclusion of two MOSFETs per cell, one for turning on the *npn* and another one for turning it off. On the positive side, the use of two gates offers more control over the *npn* and increases the switching frequency by quickly removing the stored charge on the *npn* base during turn-off. Another advantage is the similarity between the MGT and DIMOS processes, which reduces process development efforts.

3.4.1. Design

The n-channel MGT integrates a high mobility n-channel MOSFET and a *npn* bipolar transistor in a single structure, thereby realizing a high performance power device in SiC and alleviating the problem of thyristor latch-up often faced by IGBTs. The n-channel MGT is essentially an n-channel MOSFET driving an *npn* bipolar transistor, as shown in

Figure 3-57. There is an optional n-channel turn-off MOSFET integrated in the structure. For SiC, the MGT has a well-suited device structure due to the higher transconductance of n-channel MOSFET over p-channel and the higher current gain and BV_{CEO} of *npn* than the *pnp* counterpart. The *npn* is more rugged than the *pnp* in SiC because the hole ionization coefficient is larger than the electron coefficient. Since the MGT does not have a four-layer parasitic thyristor, a better forward bias SOA is expected. Furthermore, the MGT uses n+ substrate, which has much lower resistivity than the p+ substrate used for the n-channel IGBT in SiC. For all these reasons, this structure exhibits good on-state and reverse blocking characteristics as well as wider FBSOA and RBSOA. In addition, it is free from the latch-up phenomenon, which endangers IGBTs.

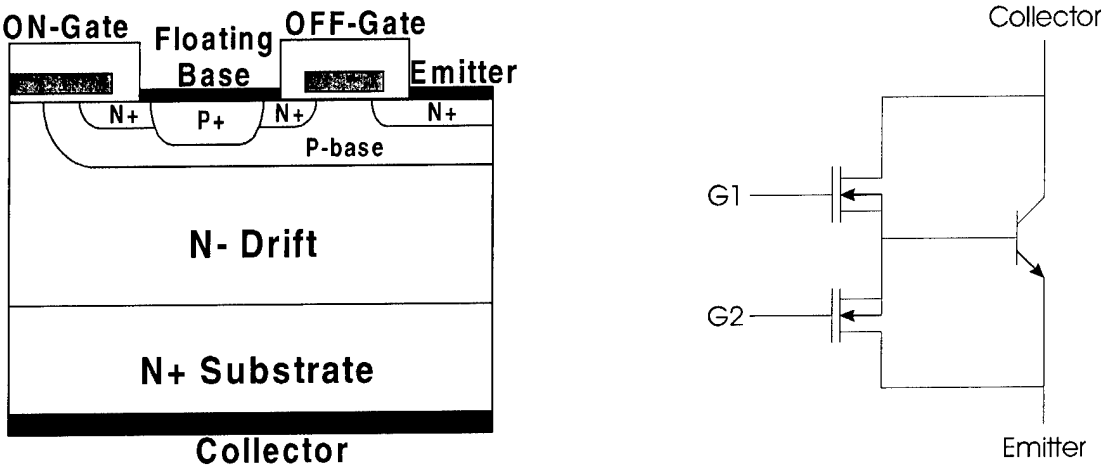


Figure 3-57. MGT cross-section and schematic

The design of a 5000 V DMOS MGT has many features in common with that of a simple DMOS. To withstand a 5000 V blocking voltage in the off-state, the doping level of the N^- drift region must be as low as possible, typically about $1\text{-}2\text{x}10^{15}$ cm^{-3}. The corresponding epi layer thickness must be about 40 μm thick. The doping and thickness of the P-base region must be tailored to the requirements of the *npn* base. It must also be wide enough to contain its share of the space charge in the blocking mode to avoid shorting the N+ source region to the drift region. Typically the P-base is doped to about $2\text{-}4\text{x}10^{17}$ cm^{-3} and is about 1-2 μm thick. The actual design parameters are derived from numerical simulations, whose results are given in the next section. Since the implementation of the preferred design parameters is often conflicting with process technology capabilities, trade-offs are necessary until the SiC technology reaches a higher level of maturity.

3.4.2. Modeling

MGT performance has been numerically simulated using carefully assessed values of the material parameters and their temperature dependence, which were extracted from experimental data. These include impact ionization coefficients, band gap energy, carrier mobility and dopant ionization energy levels.

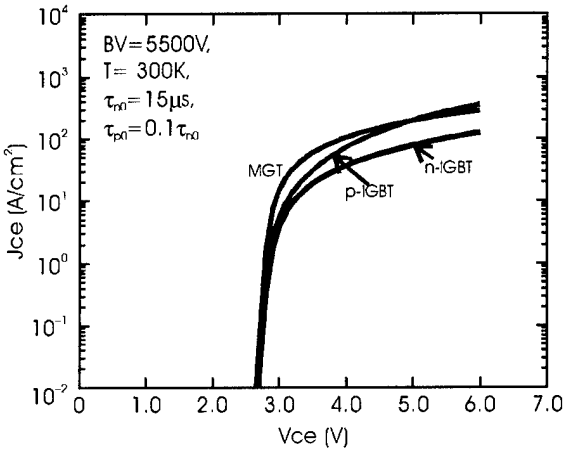


Figure 3-58. Forward I-V characteristics of 5000 V MGT, n-IGBT and p-IGBT in 4H-SiC

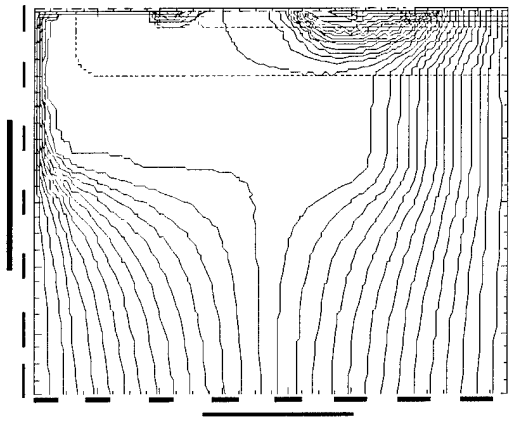


Figure 3-59. Current flow lines for 5000 V planar MGT at J=100 A/cm^2

Figure 3-58 shows the calculated forward I-V characteristics of the 5000V SiC n-channel MGT together with those of the 5000V n- and p-channel IGBTs. At room temperature the MGT forward drop is similar to that of the IGBTs. Figure 3-59 shows the current flow lines of the 5000V DMOS MGT, where one can observe that the MGT collector current is composed of the MOSFET current and the bipolar transistor current.

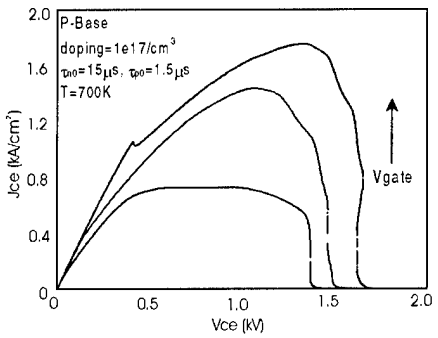


Figure 3-60. Current self-limiting effect for 5000 V SiC MGT with low p-base doping. Curves correspond to various gate voltages.

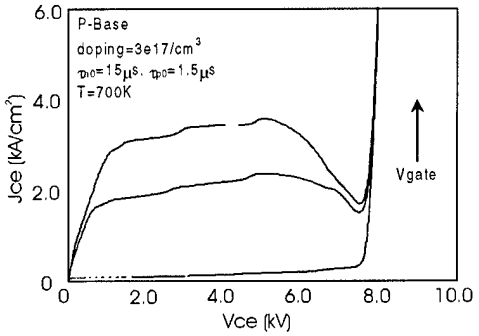


Figure 3-61. Forward-bias SOA of 5000 V MGT with optimum p-base doping. Curves correspond to various gate voltages.

A current self-limiting effect is observed when low P-base doping is used. For a 2 μm thick P-base with a doping of 1×10^{17} cm^{-3}, most of the P-base is depleted after applying a certain collector bias. In this case, the feeding path of the base current is cut off, leading to a decrease of the collector current. Figure 3-60 shows this effect using a family of curves for various gate voltages. Although this feature can serve as a protection in the on-state or over-current conditions, in the off-state, the base punchthrough will degrade the breakdown voltage if the P-base becomes wholly depleted. Therefore, it is important to choose a P-base doping concentration and thickness that prevents punchthrough across the base from occurring before the avalanche breakdown. Figure 3-61 shows the MGT forward bias SOA when using an optimal P-base doping of 3×10^{17} cm^{-3}. The MGT forward bias SOA is superior to that of the IGBT mainly because there is no parasitic thyristor and therefore no latch-up to be concerned with.

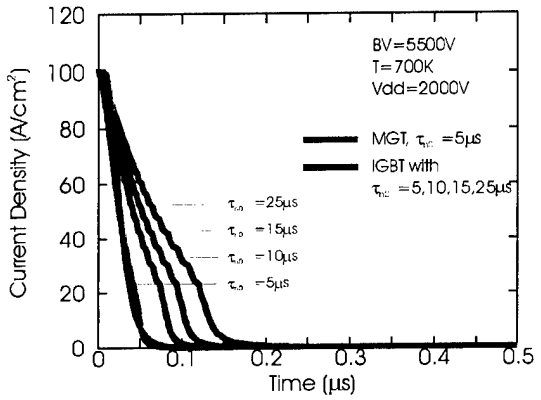


Figure 3-62. Turn-off transient of 5000 V SiC MGT and IGBT at 700 K

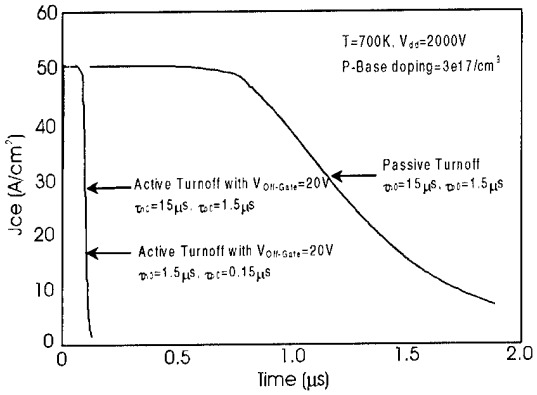


Figure 3-63. Passive and active turn-off transient of 5000 V SiC MGT at 700 K

Figure 3-62 shows the turn-off transients for the n-channel MGT and IGBT. Unlike the IGBT, the MGT turn-off characteristics are not necessarily open base and can be controlled by an integrated turn-off MOSFET. During passive turn-off, the electron and hole plasma is extracted from the drift region. In the active mode, the minority carriers are extracted out of the device through the turn-off MOSFET channel. Since the primary mechanism of the active turn-off is not recombination, the turn-off is much faster and almost independent of carrier lifetime. Figure 3-63 compares the simulated MGT active turn-off with different lifetimes and the passive turn-off.

MGTs exhibit a significant improvement in reverse-bias SOA compared to IGBTs. Figure 3-64 shows the simulated RBSOA of 5000 V SiC n- and p-channel IGBTs with non-punchthrough (NPT) and punchthrough (PT) blocking voltage region design. For comparison, Figure 3-65 shows the simulated RBSOA of a 5000 V SiC MGT. The main reason for the RBSOA difference is the narrow base and lightly doped collector of the MGT bipolar transistor. Due to the Kirk Effect, when the collector current increases, the electrons flowing into the drift region change the electric field profile in the collector, resulting in an increase of the maximum sustainable collector voltage. This effect leads to

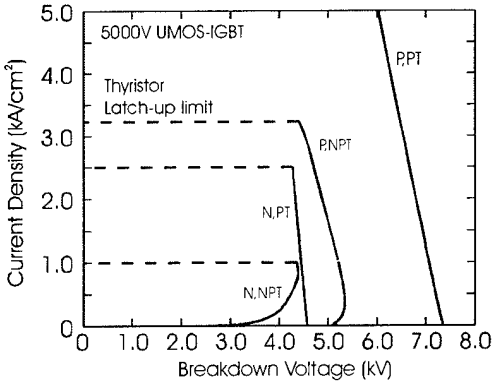


Figure 3-64. RBSOA of n- and p-channel IGBT with punchthrough (PT) and non-punchthrough (NPT) design

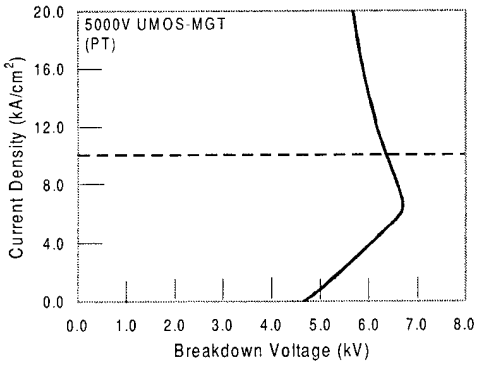


Figure 3-65. RBSOA of 5000 V SiC MGT with punchthrough (PT) design

an increase of the breakdown voltage with increasing current density in part of the MGT RBSOA, as shown in Figure 3-65. This figure also shows that the RBSOA of the MGT is wider compared with that of the IGBT.

3.4.3. Layout

1. Base-line process and design parameters:

P-base doping = 3e17 cm^{-3}	$L_{on\text{-}Gate}$ = 7 μm
N- drift layer thickness = 40 μm	$L_{off\text{-}Gate}$ = 4μm
N- drift layer doping = 1e15 cm^{-3}	W_E = 10 μm

2. Masking Layer Assignments: *(*: Align to Gate)*

Step	GDS Layer	GDS Layer Data	Digitize Data	Purpose
1	1	ALIGNMENT	CLEAR	ALIGNMENT
2	2	JTE1	CLEAR	JUNCTION
3	3	JTE2	CLEAR	JUNCTION TERMINATION
4	4	JTE3	CLEAR	JUNCTION TERMINATION
5	5	PBASE	CLEAR	DEFINE P-BASE IMPLANT REGION
6	6	PPLUS	CLEAR	DEFINE P+ IMPLANT REGION
7	7	NPLUS	CLEAR	DEFINE N+ IMPLANT REGION
8	8	ACTIVE	CLEAR	DEFINE ACTIVE AREA
9	9	GATE	DARK	DEFINE POLYSILICON GATE AREA
10	10	NCONTACT*	CLEAR	OPEN CONTACT WINDOW TO P+
11	11	PCONTACT*	CLEAR	OPEN CONTACT WINDOW TO N+
12	12	GCONTACT*	CLEAR	OPEN CONTACT WINDOW TO GATE
13	13	METAL	DARK	DEFINE GATE&SOURCE PAD AREA
14	14	PASSIVATION	CLEAR	PASSIVATION AND GATE WINDOW

3. Design Rules

These rules apply to a Karl Susse contact aligner with 2 μm resolution. To take into account the statistical nature of wafer patterning, two types of rules were generated: *aggressive* and *relaxed*. This distinction allowed a trade-off between high performance and high yield in absence of fundamental device problems. Because of this double set of rules, many items in the design rules list include two numbers corresponding to both rule types.

1. Alignment Trench

1A Minimum trench width: 3 μm

1B Minimum trench spacing: 3 μm

2. JTE1 Implant

2A Minimum overlap with p-base implant: 10 μm

2B Minimum spacing between p+ and jte1: 10 μm

3. JTE2 Implant

3A Minimum overlap with p-base implant: 10 μm

4. JTE3 Implant

4A Minimum overlap with p-base implant: 10 μm

4B Minimum spacing between n+ and jte3 edge: 30 μm

4C Total JTE width: 100 μm

5. P-plus implant

5A Minimum poly gate to p-plus edge spacing: 3 μm

5B Minimum pplus width: ***7μm vs 10μm***

6. N-plus implant

6A Minimum Gate overlap with n+ edge: ***2μm vs 3μm***

7. Active

7A Minimum field oxide overlap of p+ short: 2 μm

8. Gate

8A Minimum Gate overlap with n+ edge: ***2 μm vs 3μm***

8B Minimum Gate2 width: 6 μm

8C Minimum Gate2 overlap with n+ edge: ***2 μm vs 3μm***

8D Minimum Gate spacing: 6 μm

9. N-contact

9A Minimum spacing between poly gate and n-contact edge: 3 μm

9B Minimum n-contact to p-junction spacing: 2 μm

10. P-contact

10A Minimum p-contact to p+ edge spacing: ***2 μm vs 3μm***

10B Minimum p-contact width: ***3 μm vs 6μm***

11. Gate contact

11A Minimum gate contact to poly gate edge spacing: 2 μm

12. Metal

12A Minimum overmetal width: 5 μm

12B Minimum overmetal overlap of contact: 3 μm

12C Minimum overmetal pad size: 100 μm x 100 μm

12D Minimum metal spacing: 6 μm

13. Passivation

13A Minimum Passivation pad opening: 90 μm x 90 μm

4. MGT design variants

The MGT mask set contains an array of devices with various design variations with respect to the baseline. These variants include the most important layout parameters that need to be optimized through simulation and experimental verification. The parameter dimensions in the table below are expressed in μm. The maximum device size is 1.2 mm x 1.2 mm to be consistent with an acceptable yield, given the high defect density of the starting material. The ratio G:E expresses the gate electrode to emitter ratio.

Size	With or w/o Gate2	Gate2 channel length	Gate1 Channel length	p-base to p-base	G:E	Name
1200x1200	with	8	7	10	1:1	S12A
1200x1200	with	4	7	10	1:2	S12B
1200x1200	with	2	5	6	1:2	S12C
1200x1200	with	4	12	10	1:1	S12D
1200x1200	w/o	N.A.	10	8	1:1	S12E
1200x1200	with	4	10	8	1:2	S12F
800x800	with	4	7	10	1:1	S8A
800x800	w/o	N.A.	7	10	1:1	S8B
800x800	with	2	3	6	1:1	S8C
800x800	with	4	10	10	1:2	S8D
800x800	w/o	N.A.	5	8	1:1	S8E
800x800	with	4	5	10	1:2	S8F

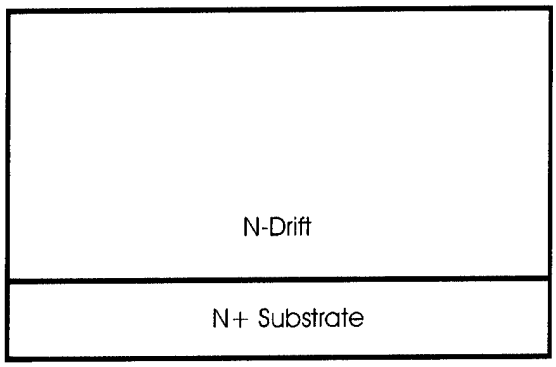
5. Electrical Test Element Group

A test element group (TEG) has been included in the mask set for process diagnostic purpose. The TEG elements were selected to provide measurements of the individual device components, which are integrated in the MGT cell. With this information the MGT performance can be evaluated against the simulations by using realistic input parameters.

1. NMOS Capacitor
2. PMOS Capacitor
3. NPN BJT
4. Lateral PNP BJT
5. Device size BJT
6. MOSFETs
7. Hall Structure: Pbase, Nplus, Pplus, JTE
8. Pplus-Nepi Diodes
9. Pbase_Nepi Diodes
10. NMOS and PMOS Gated Diodes
11. Van de Pauw for sheet resistance
12. Kelvin 6-Terminal Contact resistance
13. Circular TLM: NCONT, PCONT
14. Linear TLM: NCONT, PCONT

3.4.4. Fabrication

The MGT fabrication process is described below with device cross-sections at critical phases of the process, accompanied by a list of the corresponding processing steps. Unfortunately, technical problems encountered in MOS processing and premature exhaustion of program funds have prevented us from fabricating these devices during the Megawatt program. The possibility of this decision was considered from the beginning of the program, because the MGT was a secondary approach for a 3-terminal switch as an alternative to the 5000 V GTO.



Starting Material
4H-SiC N+ substrate
Epi layer: N-type, 2-4e15 cm^{-3}

Trench Alignment Key (level-1)
Solvent clean
Karo's clean, RCA clean
Deposit oxide (1.5 μm)
Densify oxide
Pattern trench (level-1)
RIE (oxide, SiC, 0.5 μm)
Strip oxide
Strip resist

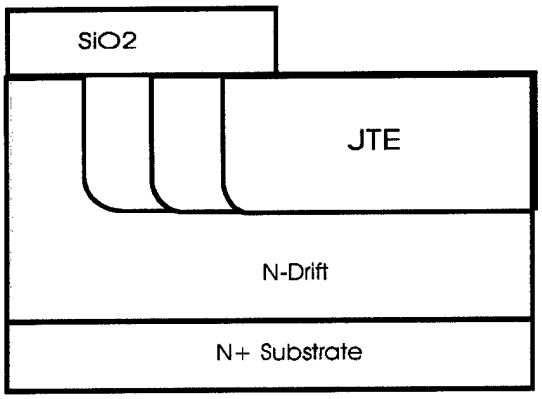
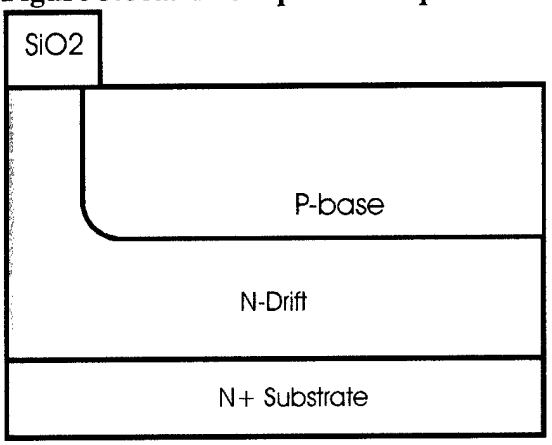
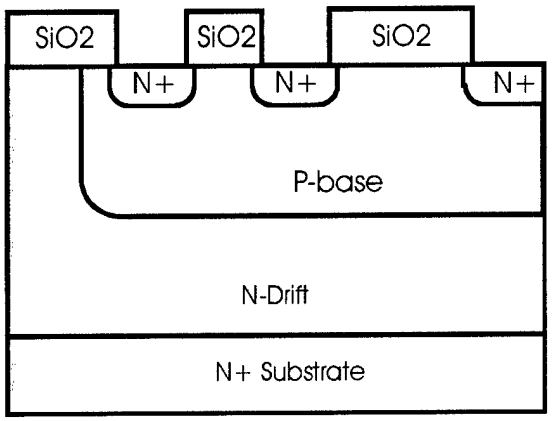


Figure 3.66a. MGT process sequence.

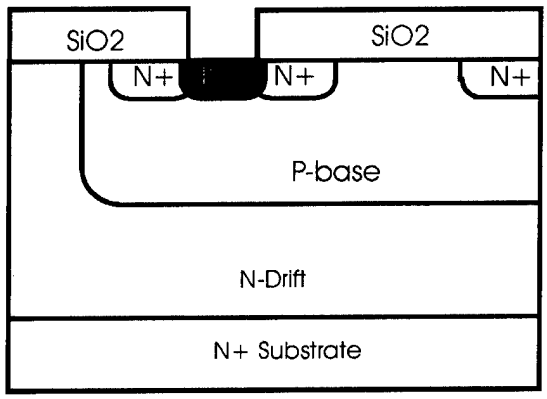
JTE implant (level-2,-3,-4)
Clean
Deposit oxide (10,000 Å)
Densify oxide
Pattern JTE-1 (level-2)
Etch oxide (10,000 Å, to bare SiC)
Strip resist
Deposit screen oxide (500 Å)
Boron implant
Strip oxide
Repeat for JTE-2, -3 (level-3,-4)



P-base implant (level-5)
Clean
Deposit oxide (20,000 Å)
Densify oxide
Pattern P-base (level-5)
Etch oxide
Strip resist
Deposit screen oxide (500 Å)
B implant (650 °C), 3e17cm^{-3} at least 1.5 µm deep)
Strip oxide

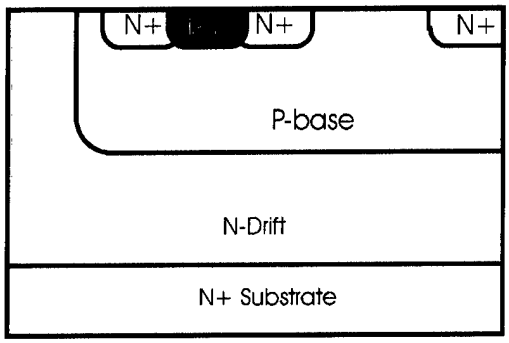


N$^+$ implant
Clean
Deposit oxide (20,000 Å)
Densify oxide
Pattern nplus (level-6)
Etch oxide
Strip resist
Deposit screen oxide (500 Å)
P implant (650 °C)
Strip oxide



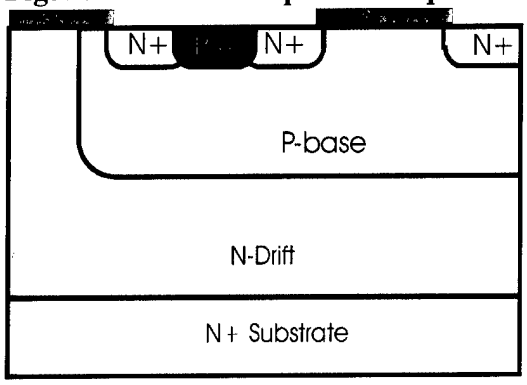
P+ implant
Clean
Deposit oxide (20,000 Å)
Densify oxide
Pattern pplus (level-7)
Etch oxide
Strip resist
Deposit screen oxide (500 Å)
Boron implant
Strip oxide

Implant activation anneal

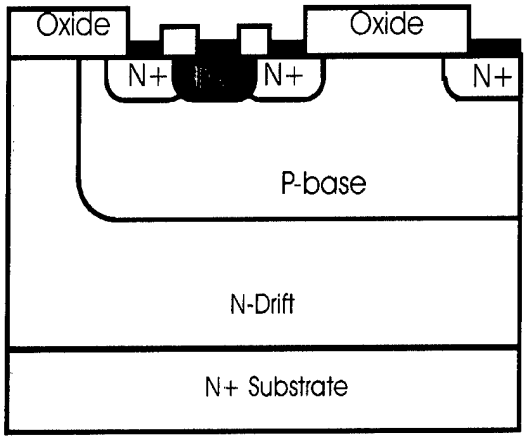


Active area definition
Clean
Sacrificial oxide growth
Etch sacrificial oxide
Field oxide
Pattern active area (level-8)
Etch oxide to bare SiC with overetch
Strip resist

Figure 3.66b. MGT process sequence.



Gate formation
Clean
Gate oxide (1000 Å)
Deposit polysilicon
Dope polysilicon
Pattern gate electrode (level-9)
Etch polysilicon
Strip resist



P-contact
Clean
Deposit HTO (6000 Å)
Coat frontside with PR
Remove backside polysilicon and oxide
Pattern P-contact (level-10)
Wet etch oxide (6000 Å)
Deposit P-contact metal stack
Lift-off resist

N-contact
Pattern N-contact (level-11)
Wet etch oxide (6000 Å)
Deposit N-contact metal stack
Lift-off resist
Deposit N-contact metal on the backside

Contact metal anneal (1050 °C, 2 min)

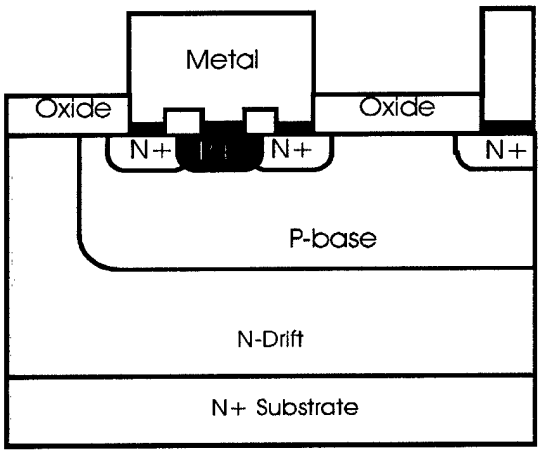


Figure 3.66c. MGT process sequence.

Gate contact
Pattern gate contact (level-12)
Etch oxide
Strip resist
Solvent clean

Metallization
Deposit Ti/Mo (2000 Å/4000 Å)
Deposit backside metal
Ti/Mo/Au (2000 Å/4000 Å/2000 Å)
Pattern metal (level-13)
Etch metal
Strip resist

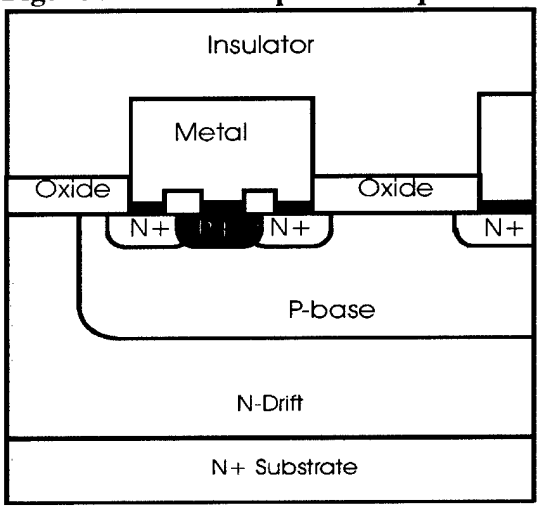


Figure 3.66d. MGT process sequence.

Passivation
Solvent clean
Deposit LTO (10,000 Å)
Pattern bonding pads (level-14)
Etch LTO
Strip resist

3.5. RPI publications with Megawatt program support

3.5.1. Journal Articles

(1) N. Ramungul, V. Khemka, R. Tyagi, T.P. Chow, M. Ghezzo, P.G. Neudeck, J. Kretchmer, W. Hennessy, and D.M. Brown, "Comparison of Aluminum- and Boron-Implanted Vertical 6H-SiC p^+n Junction Diodes," Solid-State Electronics, 42, 17-22 (1998).

(2) N. Ramungul, and T.P. Chow, "Current-Controlled Negative Resistance (CCNR) in SiC P-i-N Rectifiers," IEEE Trans. Electron Devices, 46, 493-496 (1999).

(3) V. Khemka, R. Patel, N. Ramungul, T.P. Chow, M. Ghezzo, and J. Kretchmer, "Characterization of Phosphorus Implantation in 4H-SiC," J. Electron. Mat., 28, 167-174 (1999).

(4) V. Khemka, T.P. Chow, and R.J. Gutmann, "Design Considerations and Experimental Analysis for Silicon Carbide Power Rectifiers," Solid-State Electronics, 43, 1945-1962 (1999).

(5) Y. Gao, Y. Tang, M. Hoshi, and T.P. Chow, "Improved Ohmic Contacts on n-type 4H-SiC," Solid-State Electronics, 44, 1875-1878 (2000).

(6) T.P. Chow, V. Khemka, J. Fedison, N. Ramungul, K. Matocha, Y. Tang, R.J. Gutmann, "SiC and GaN bipolar power devices, "Solid-State Electron., vol.44, no.2 p. 277-301, Feb, 2000.

(7) V. Khemka, V. Ananthan and T.P. Chow, " A fully planarized 4H-SiC Trench MOS Barrier Schottky (TMBS) Rectifier," Solid-IEEE electron device letters, 21, 286-288, no. 5, May, 2000.

(8) Y. Tang, J.B. Fedison and T.P. Chow, "An implanted-emitter 4H-SiC bipolar transistor with high current gain, " IEEE Electron Device Letters, Vol 22, 119-120, no. 3, March, 2001.

(9) J.B. Fedison, N. Ramungul, T.P. Chow, M. Ghezzo and J.W. Kretchmer, "Electrical characteristics of 4.5 kV implanted anode 4H-SiC PiN junction rectifiers, " IEEE Electron Device Letters, Vol 22, 130-132, no. 3, March, 2001.

3.5.2. Conference Papers (Extended Abstract in Proceedings)

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(2) R. Patel, V. Khemka, N. Ramungul, T.P. Chow, M. Ghezzo, and J. Kretchmer, "Phosphorus-Implanted High-Voltage N^+P 4H-SiC Junction Rectifiers," Proc. 10th International Symp. Power Semiconductor Devices and ICs, pp.387-390, Kyoto, Japan, May 3-6, 1998.

(3) N. Ramungul, V. Khemka, T.P. Chow, M. Ghezzo, J. Kretchmer, "Carrier lifetime extraction from a 6H-SiC high voltage p-i-n rectifier reverse recovery waveform", International Conference on Silicon Carbide and Related Materials, Stockholm, Sweden; 31 Aug.-5 Sept. 1997

(4) V. Khemka, R. Patel, N. Ramungul, T.P. Chow, and R.J. Gutmann, "Static and Dynamic Characteristics of a 1100V, Double-Implanted, Planar, 4H-SiC PiN Rectifier," Proc. 11th International Symp. Power Semiconductor Devices and ICs, pp.137-140, Toronto, Canada, May 26-28, 1999, IEEE Catalog Number: 99CH36312.

(5) V. Khemka, V. Ananthan, and T.P. Chow, "A 4H-SiC Trench MOS Barrier Schottkly (TMBS) Rectifier," Proc. 11th International Symp. Power Semiconductor Devices and ICs, pp.165-168, Toronto, Canada, May 26-28, 1999, IEEE Catalog Number: 99CH36312.

(6) Y. Tang, N. Ramungul, and T.P. Chow, "Design and Simulations of 5000V MOS-Gated Bipolar Transistor (MGT) on 4H-SiC," International Conference on Silicon Carbide and Related Materials, Research Triangle Park, NC, Oct. 10-15, 1999.

(7) J.B. Fedison, T.P. Chow, M. Ghezzo, J. W. Kretchmer, M. C. Nielsen, "Factors influencing the design and performance of 4H-SiC GTO thyristors", International Conference on Silicon Carbide and Related Materials, Research Triangle Park, NC, Oct. 10-15, 1999.

(8) Z. Li, J.B. Fedison, V. Khemka, N. Ramungul, T.P. Chow, M. Ghezzo, J. Kretchmer, and A. Elasser, "Al/C/B Co-Implanted High Voltage 4H-SiC PiN Junction Rectifiers," International Conference on Silicon Carbide and Related Materials, Research Triangle Park, NC, Oct. 10-15, 1999.

(9) K. Matocha, T.P. Chow, and R.J. Gutmann, "Non-Contact Characterization of Recombination Processes in 4H-SiC," Paper T4.4, Materials Research Society Spring Meeting, San Francisco, CA, April 24-28, 2000.

(10) J.B. Fedison and T.P. Chow, "Characteristics of Epitaxial and Implanted N-Base 4H-SiC GTO Thyristors," WeP-77, Third European Conference on Silicon Carbide and Related Materials (ECSRM 2000), Kloster Banz, Germany, Sept. 3-7, 2000.

3.5.3. Conference papers (Only abstract in Proceedings)

(1) R.K. Patel, V.K. Khemka, T.P. Chow, M. Ghezzo, and J. Kretchmer, "Characterization of Phosphorus Implantation in 4H-SiC," Paper K8, presented at the Electronics Materials Conference, Univ. of Virginia, Charlottesville, VA, June 24-26, 1998.

(2) J.B. Fedison, Z. Li, N. Ramungul, T.P. Chow, M. Ghezzo, and J. Kretchmer, "4500V Planar Implanted Anode p-i-n Junction Rectifiers in 4H-SiC," Device Research Conference, June, 1999.

(3) V. Khemka, T.P. Chow, and R.J. Gutmann, "Characteristics of Nickel Schottky Junctions on Trench Sidewalls of Reactive Ion Etched 4H-SiC Surfaces," Electronics Materials Conference, Santa Barbara, CA, June, 1999.

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(5) Z. Li, L. Zhu, and T.P. Chow, "N-type Doping of 4H-SiC with Phosphorus Co-implanted with C, Si and N," Paper Q7, Electronic Materials Conference, Denver, CO, June 21-23, 2000.

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(1) T.P. Chow, "Wide Bandgap Semiconductor High-Voltage Power Switching Transistors," (INVITED) Abstr. No. 567, Meeting Abstracts, vol. 98-2, Electrochem. Fall Meeting, Boston, MA, Nov. 1-6, 1998.

(2) T.P. Chow, "SiC and GaN High-Voltage Power Switching Devices," International Conference on Silicon Carbide and Related Materials, Research Triangle Park, NC, Oct. 10-15, 1999.

(3) T.P. Chow, "SiC High-Voltage Power Switching Devices," Japanese Conference on Silicon Carbide, Tsukuba, Japan, Dec. 16-17, 1999.

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Proceedings of International Symposium on Power Semiconductor Devices & ICs, 1998, pp. 127 - 130.

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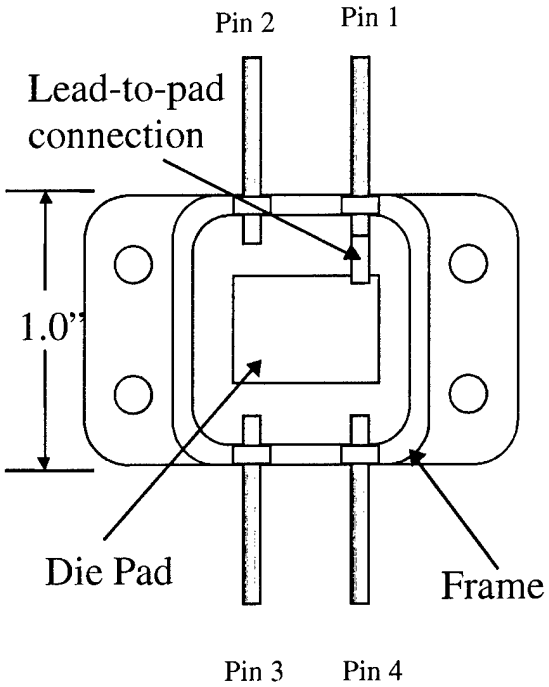
4. Packaging

Packaging is an integral part of power device development, because it enables to retain and transfer the power device properties to the system level. Specifically, for the SiC megawatt program, packaging technology must provide high voltage isolation, high current leads, high temperature operation and high frequency switching with minimal waveform distortion. These requirements are well beyond the capabilities of the present packaging technology and must be addressed with a focused R&D program. However, due to partitioning of the DARPA megawatt program among various contractors, packaging technology development was not funded at GE. Therefore, because of limited resources, we restricted our packaging effort to the support of the device development needs with full recognition that this was only an intermediate packaging milestone. Two packaging activities were entertained. One was discrete device packaging for enabling characterization of SiC devices at high temperature and high voltage without the wafer-probe testing restrictions. Another one was the development of an integrated power module for encasing a hybrid Si/SiC half-bridge inverter with low parasitics. The latter also served to achieve with SiC a high level of integration comparable to Si and to evaluate the difference between these semiconductors in power applications on an even base. A discussion of these developments is presented in the next sections.

4.1. Discrete packaging

The discrete package design was based on the specifications of the SiC diodes and GTOs, which were produced under the Megawatt program. Therefore, the packaging characteristics that were emphasized were high temperature to 350 °C and high voltage to



Manufacturer
Sinclair Mfg., Chartley, MA

Features
- Frame⇒ Steel
- Seal ⇒ Glass
- Leads ⇒ 52 Alloy, Cu Core
- Base ⇒ Steel
- Pad ⇒ BeO
- Large isolation between lead and frame
- Large distance between lead ends and pad

Figure 4-1. Design and properties of 5000 V discrete package.

5000 V. On the other hand, the terminal leads were designed for a maximum current of 20 A in agreement with the maximum chip area and expected current density. Moreover, any further current rating increase would have also required a change from wire bonding to less conventional top contact techniques, such as pressure contact with large metal bumps or metal ribbon. Figure 4-1 shows the key characteristics of the discrete package.

This package is a modified TO-254 model for use in aerospace applications. Sinclair Manufacturing Company, Chartley, MA developed it in conjunction with the packaging group of Lockheed Martin Control Systems, Fort Wayne, IN. It consists of a low-profile gold-plated metal case with a large baseplate and a top metal lid to hermetically seal the package. Four metal leads penetrate inside the case through electrically isolated feedthru holes located on opposite sides of the frame. Three leads are completely isolated, while the fourth lead is internally connected to an isolated bottom pad, used for die attachment. The ceramic insulator sandwiched between the die pad and the metal case is made of BeO. The leads have a copper core and are plated with a metal forming a thermally stable alloy with the bonding wires. The package footprint measures 1" x 1" and is therefore capable to accommodate even the largest SiC power devices of the present generation while maintaining a safe electrical isolation within the package up to 5000 V. Multiple photographs of the package with and without the lid are shown in Figure 4-2.

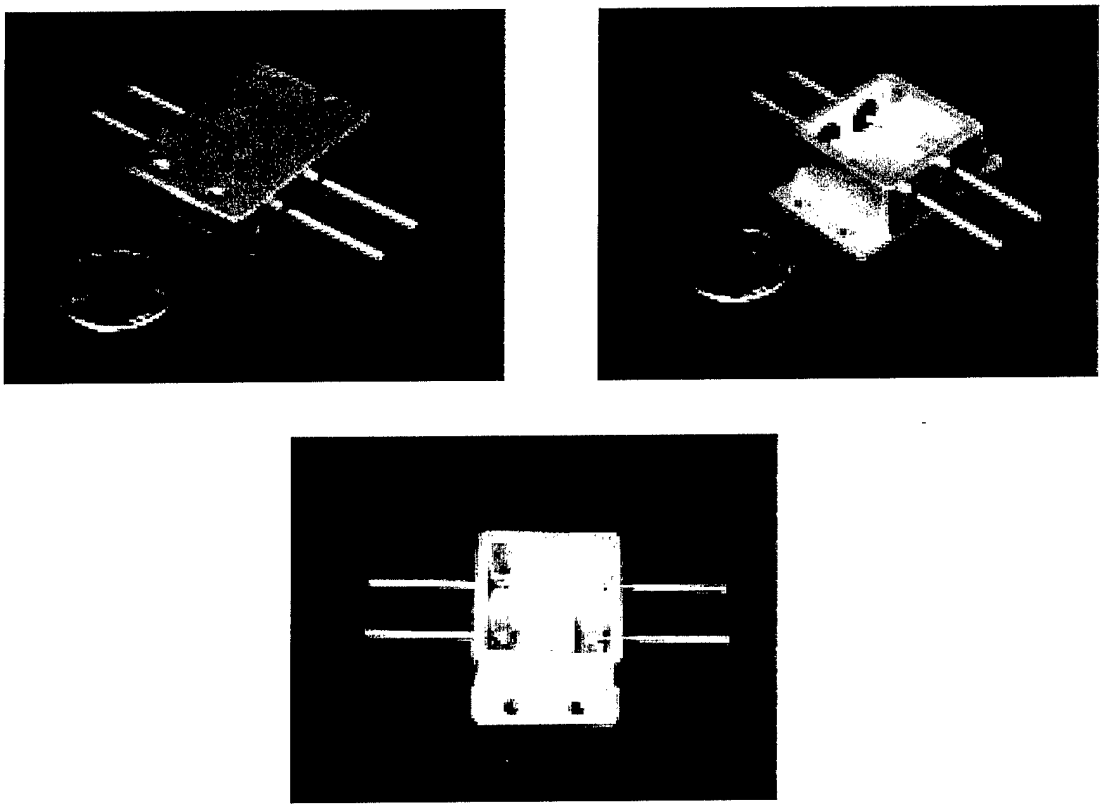


Figure 4-2. Multiple views of the discrete package.

The package development proceeded through several iterations with intermediate reliability tests at the maximum temperature and voltage specifications. As a result of these tests and related failure analysis several changes were made. One change consisted of increasing the ceramic isolation barrier between the leads and the feedthru holes, because high leakage was observed in the package at this location under concurrent voltage and thermal stress. In addition, the distance from the leads to the die attach pad was also increased because arching between these parts occurred frequently at the maximum voltage rating causing a catastrophic failure.

GECRD and Lockheed Martin Control Systems jointly developed the packaging process. A new die attachment process replaced a low melting point Sn/Pb solder used for Si with a brazing technique based on Au/In alloy with melting point > 350 °C. The die metallization also changed to withstand high temperature operation. We used a Ti/Mo/Au stack for the bonding pads and Ti/Pt/Au for the backside. This metallization is compatible with gold wiring. Although this system performed well for currents up to 1 A using multiple gold wires on each pad, it failed at higher currents due to thermal run-away caused by resistance heating on the wires. Since thicker (>3 mil diameter) gold wires were not readily available, we switched temporarily to an aluminum wiring system with multiple 8 mil diameter Al wires and top Al contacts. With this system we were able to test the devices up to 15 A, but at a lower temperature (250 °C).

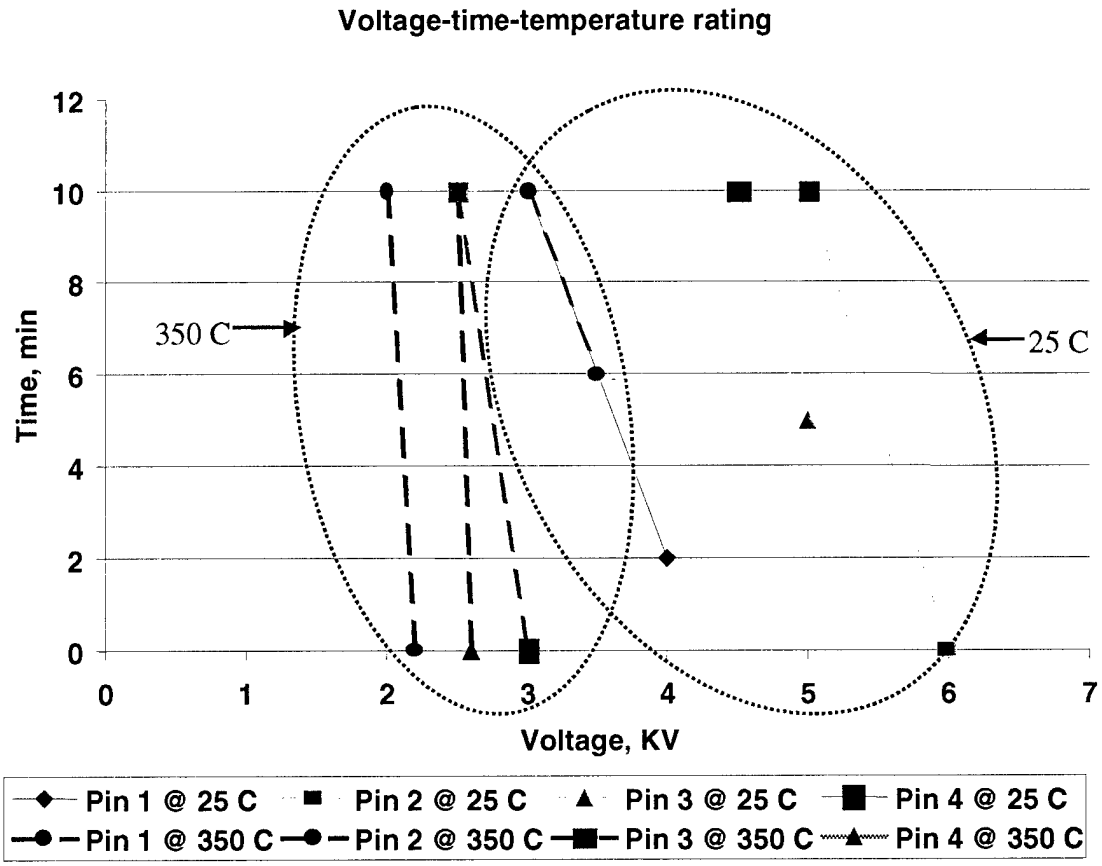


Figure 4-3. Test results on discrete package.

The package alone was stress-tested for various times in a small oven at high temperature and high voltage to determine the upper limits of these parameters. Figure 4-3 shows the results of these tests. The vertical axis represents the time scale in minutes while the horizontal axis represents the applied voltage in kilovolts. The data points have different shape and color to distinguish the pin number and testing temperature. Lines connect data for the same pin number and temperature, but different stress time and voltage.

Each pin was measured separately to account for geometrical configuration differences among pins within the package and consequent electrical isolation dependence with respect to ground, represented by the baseplate. Since these tests were made without sealing the package in vacuum, the results represent the worst case due to lower dielectric strength of air compared to vacuum and presence of ionized particles in air. The data points correspond to the voltage, temperature and time conditions, for which the leakage current rises above 1 μA at the pin under test. This is an indication of an incipient isolation failure, either due to insulator damage or electrical discharge across the air gap between pin and ground.

The test sequence was designed for conducting all the tests using at most two packages, one at 25 °C and the other at 350 °C, because of the destructive nature of these tests. For each temperature and pin, the voltage was increased in steps of 0.5 kV checking the leakage periodically and waiting a maximum of 10 min before applying another voltage increment. The stress causing conditions of time and voltage explain the negative slope of the majority of the lines in Figure 4-3, because at the approach of isolation failure conditions either an increase of voltage or time determines this event. As expected, all pins have a higher withstanding voltage at 25 °C (> 3 kV) than at 350 °C (>2 kV). Since the electrical test was not followed by a physical failure analysis, the mechanism and location of the failures have not yet been determined. Unfortunately, these results show that the 5 kV design specifications of this package have not yet been achieved, although before reaching this conclusion this test should have been repeated with a vacuum sealed package.

Despite the fact that the SiC diodes produced in this program have a breakdown voltage higher than the above package ratings, this discrete package permits improved testing of the diode and GTO switching characteristics and provides useful data for improving successive versions of this package.

4.2. Integrated package module

Since power device circuits often include standard building blocks, it is customary to package them into integrated modules to reduce circuit parasitics, particularly stray inductance, and to expedite circuit assembly. The most common building block is the combination of a 3-terminal switching device, such as an IGBT, and an antiparallel flyback diode. Since application engineers are accustomed to design with these modules, the availability of these modules with SiC components will facilitate the acceptance of SiC power device technology. As discussed in chapter 3, the snapback-free fast switching characteristics of SiC diodes are ideal for this application, whose circuit

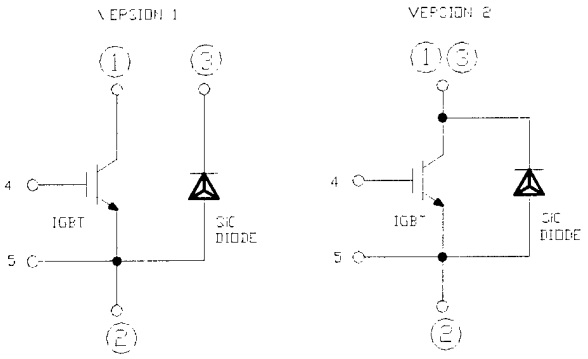


Figure 4-4. Integrated module circuit diagram.

schematic is shown in Figure 4-4. GE and Powerex teamed together under the Megawatt program to implement this integrated module by modifying a current Powerex product, which contains only Si devices. Two versions were developed. In version 1, the Si IGBT collector is connected to a separate terminal from the SiC cathode to give the designer more flexibility. For instance, this configuration allows the insertion of a current measuring device in series with either the IGBT or the diode. In version 2, these terminals are hardwired together inside the package, although for facilitating external wiring terminals 1 and 3 are two physically different terminals located on opposite sides of terminal 2 in the package. While the above terminals are sized to carry large currents, terminals 4 and 5 are smaller, because they carry the voltage signals from the gate driver to the IGBT.

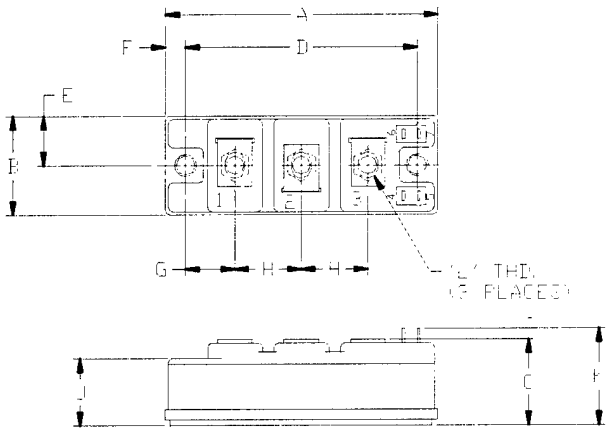


Figure 4-5. Integrated module outline drawing.

The drawing outline of the integrated module is shown in Figure 4-5. The package measures 9.4 mm x 3.4 mm x 3.0 mm. Terminals 1 to 3 are located in line on top of the package and are fitted with a hex nut. Terminals 4 and 5 are two small pins located at the right end of the package. At both ends there are holes in recessed regions for mounting the package to its baseplate and therefore provide a thermally conductive path for heat dissipation. Figure 4-6 shows an external view of the integrated module with the molded plastic encapsulation and the terminal connections.

The module components are a Powerex 600 V, 75 A single chip Si IGBT and a set of 6 GECRD SiC PiN diodes connected in parallel to yield 600 V, 20 A ratings. The SiC dies measure 800 μm x 800 μm and were built on 5 μm thick epi. Figure 4-7 shows a drawing

Figure 4-6. Photograph of integrated module.

of the element assembly with a corresponding list of the main items. An AlN ceramic layer is directly bonded to a copper baseplate, which forms the mechanical support of the package. The SiC diode is located on the left side, while the Si IGBT is on the right side. They are die-attached to separate metal-plated pads, which extend to terminals 1 and 3, respectively. In version 2, these pads are shorted together by Al wires, as explained earlier. The center electrode, represented by

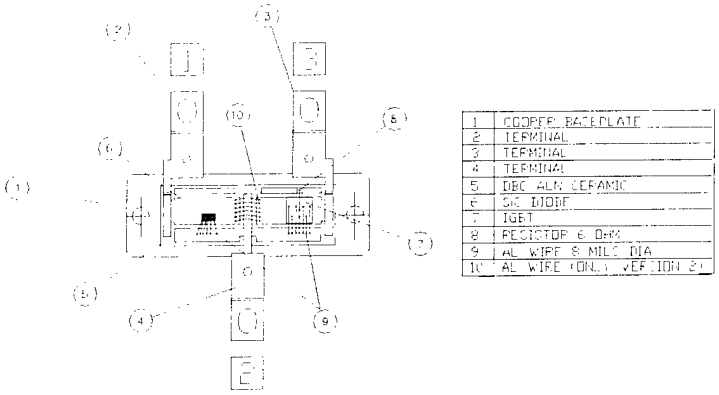


Figure 4-7. Assembly elements of integrated module.

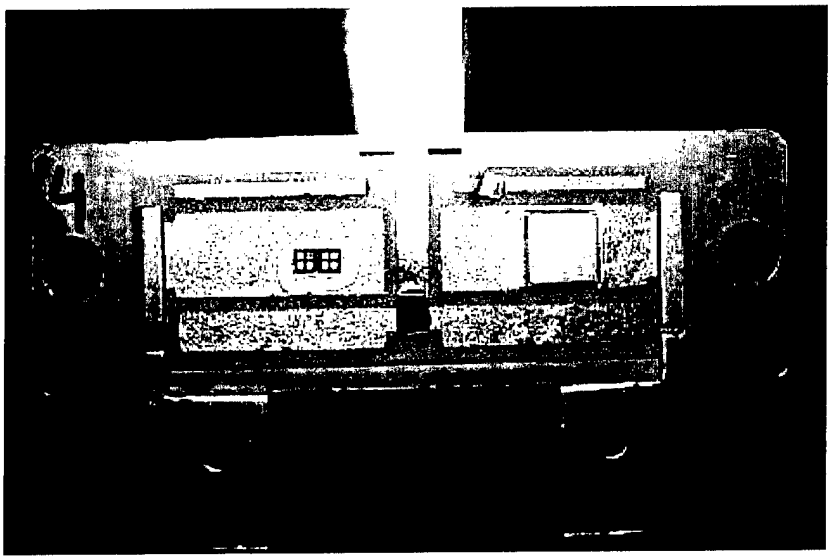


Figure 4-8. Integrated module after die attach.

terminal 2, is connected to both the IGBT emitter and the diode anode using multiple Al wires of 8 mil diameter. Figure 4-8 shows a view of the module under construction after die attach, which closely resembles the drawing of Figure 4-7. Figures 4-9 and 4-10 show the module after the next step, which is wire bonding, for version 1 (without internal connections between terminals 1 and 3) and version 2 (with wire bonding connections between the corresponding pads), respectively. Before applying the final encapsulation, the gate control leads are wired to pins 4 and 5, and the main terminal electrodes are bent upwards to reach their final position over the module. A protective insulating gel is applied over the module to form a barrier against contamination and to prevent arching. After these steps the "gelled" modules appear as shown in Figure 4-11.

Figure 4-9. Integrated module after wire bonding (version 1).

Figure 4-10. Integrated module after wire bonding (version 2).

A hard-switched pulse width modulated (PWM) full bridge inverter was developed using four integrated hybrid Si/SiC modules. Figure 4-12 shows the schematic of this circuit, which includes a high frequency leg switching at F_s=20 kHz (left side) and a low frequency leg switching at F_{load}=2 kHz (right side). The bus voltage was V_{dc}=150 V. The load parameters were R_{load}=**12.5 Ω and** L_{load}=1 mH. Thanks to the availability of integrated modules the PWM inverter circuit could be laid out with minimal space using a laminated bus card, which ensured very low inductance and therefore low stress caused by di/dt effects. The bus card layout is shown in Figure 4-13, where the outline of the

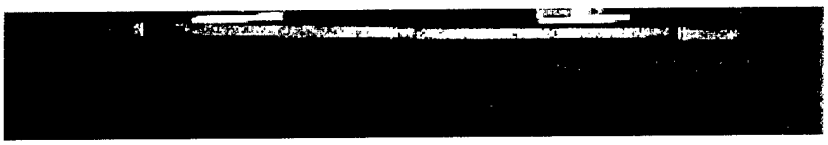


Figure 4-11. Integrated modules with gel coating and IGBT gate control wiring.

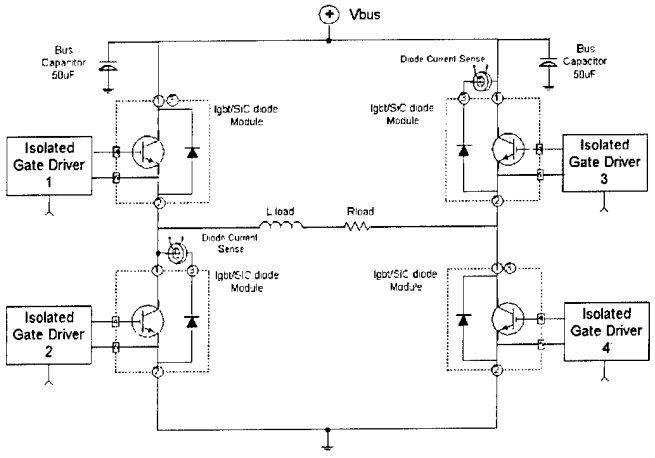


Figure 4-12. Schematic of full bridge PWM inverter.

four integrated modules is marked with dotted lines and the numbers refer to the terminal labels. The positive bus rail is color-coded in red, the negative in green, and the interconnections in yellow. The compact layout of this bus card is a clear demonstration of the fabrication advantage and high-density design achieved with the use of integrated modules. A photograph of the completed inverter, which is shown in Figure 4-14, gives further evidence of this advantage. Except for few additional components, the inverter top surface is formed by the smooth plane of the bus card, from which the hex terminals

of the four modules protrude slightly. This inverter was thoroughly tested under various switching waveforms. The results are briefly discussed in Chapter 5 in the section on the hybrid inverter application.

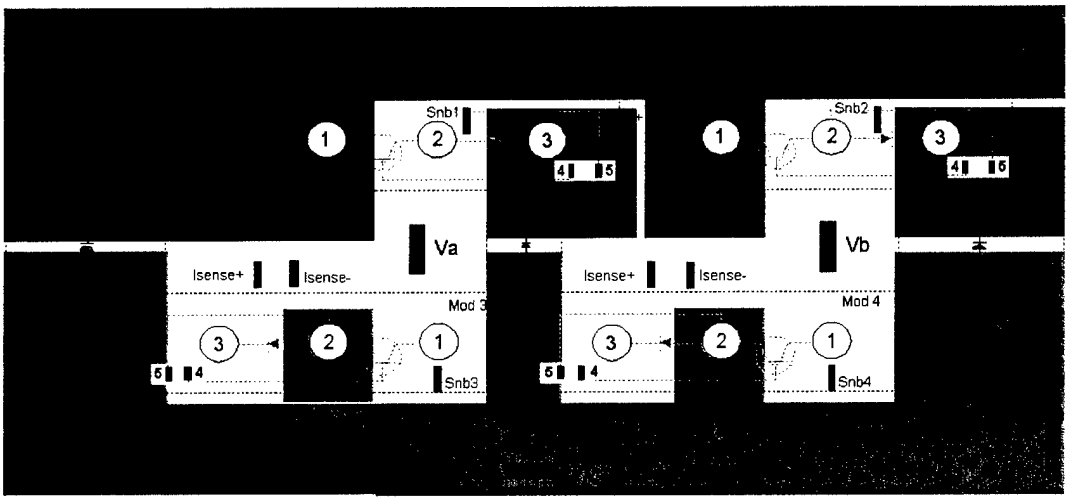


Figure 4-13. Layout of laminated bus board for PWM inverter.

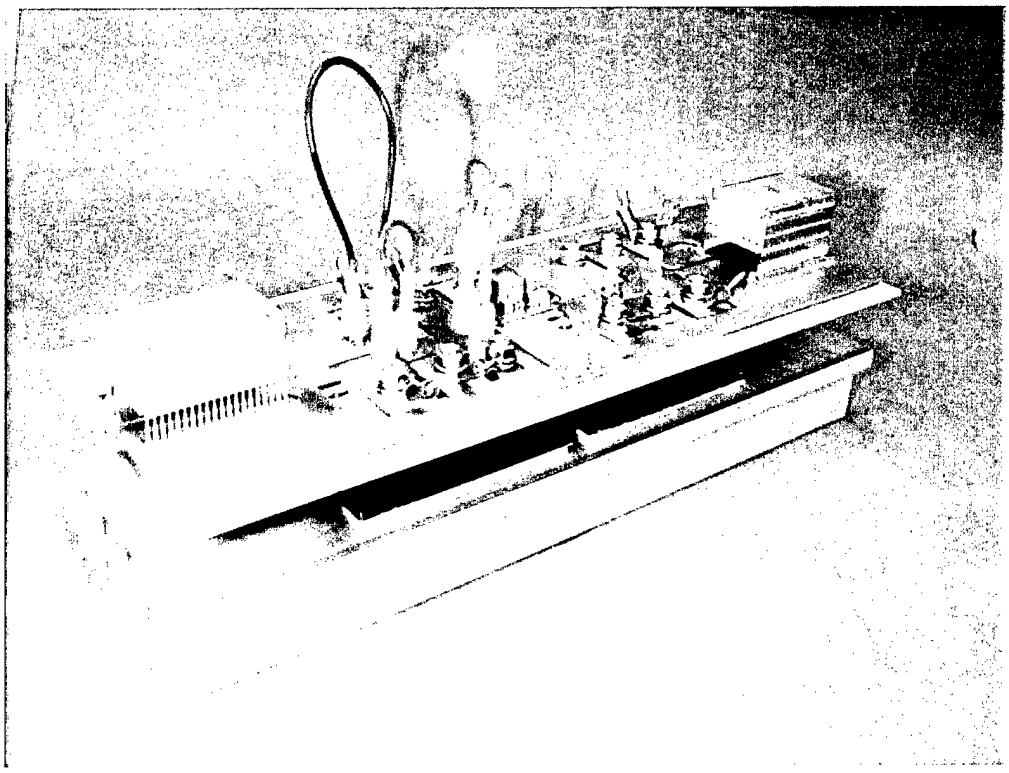


Figure 4-14. Complete PWM full-bridge inverter.

5. Applications

The advantages of SiC power electronics have been recognized long time ago on the basis of the physical properties of this semiconductor. However, until recently, the device quality and most of all the current rating have been too low for any power electronic application of even the simplest SiC device, that is a diode.

Since the material quality and cost affect all the SiC electronic applications, there has been a concerted effort by the government and industry to quickly overcome this problem. Major achievements have been the reduction of defect density below 1 def/cm^2 and the increase of wafer diameter size to 2" and soon to 3". Hence, a chip size of up to 0.5 cm^2 is becoming practical in terms of device yield, resulting in devices with current rating of up to 50 A. In addition, a voltage rating increase of up to 8.5 kV has resulted from progress in SiC epitaxy with deposition of lightly doped layers up to 70 μm thick.

Recently SiC diodes of various types have been produced with the above ratings at acceptable yields using conventional semiconductor processing equipment and facilities with only minor modifications. The Megawatt program at GE and other contractors has contributed significantly to reach this production-ready phase of SiC power electronics by developing and fabricating prototype diodes and GTOs. The availability of prototypes has enabled a complete static and dynamic characterization of device properties, which is a key factor for evaluating potential applications [1-5].

5.1. SiC applications overview

The realm of SiC power device applications is determined by several factors, such as current deficiencies of Si power devices in selected applications and opportunities for achieving higher performance and efficiency in existing or novel power systems using SiC. While SiC enjoys superior physical properties, Si is already well entrenched with a large application base and a very mature, lower cost technology. Therefore, candidate SiC power device applications are evolving in response to SiC technology progress above the reach of Si technology and by market demand for power circuit characteristics that are uniquely met by SiC.

To rationalize the best application prospects of SiC power devices it is useful to briefly review the advantages with the understanding that their relative importance will depend on the specific application. A key advantage of SiC bipolar devices is a much faster switching characteristics with a soft recovery mode and minimal temperature sensitivity. The SiC diode reverse recovery time is up to one tenth smaller than that of ultrafast silicon diodes, because of low stored charge and low carrier lifetime in SiC. Additionally, since the peak reverse recovery current is small, the energy dissipation at every switching cycle is also small resulting in higher efficiency at high switching speed. A complementary bonus is that these benefits are also matched by lower static power dissipation for high voltage SiC devices in contrast with Si ultrafast diodes, which pay a penalty for achieving high speed with a significant increase of forward voltage drop [2].

Another very important advantage of SiC is a critical electric field value nearly 10x higher than in Si, which allows a simultaneous reduction of blocking layer thickness and increase of doping concentration with consequent vertical resistance reduction by nearly 100x [2]. Since for high voltage devices, the blocking layer resistance predominates in the on-state, this resistance reduction causes a decrease of the static power dissipation with a corresponding efficiency increase from 82% to 88% compared to Si [2]. Therefore, for high voltage devices, SiC is superior to Si in terms of both static and dynamic power dissipation.

The maximum voltage of an application is an important selection criterion for the choice of SiC or Si devices on the basis of performance. The reason is that in power devices vertical conduction is affected by the substrate resistance, which in SiC at 25 °C is up to 100x higher than in Si due to partial carrier freezeout, lower dopant concentration and reduced mobility. Since the substrate resistance is voltage independent while the blocking layer resistance increases with voltage, a cross-over point divides the regions of lower specific on-state resistance achievable with Si or SiC for a given blocking voltage. Depending on the assumptions, this cross-over point is typically set at about 3 kV [6]. Nevertheless, even below this point, the choice of SiC can still be justified for high frequency and/or high temperature operation, because of soft recovery with minimal stored charge and consequent superiority in reducing switching power dissipation.

High temperature operation was one of the first SiC attributes to drive the development of this technology. This advantage is the concomitant effect of the SiC wide bandgap (3.26 eV for 4H-SiC), which results in lower reverse diode leakage current, and of about 3x higher thermal conductivity than Si, which allows a higher heat dissipation rate for a given junction temperature. The benefits of this feature extend to a variety of harsh environment applications, such as gas turbines, oil well drilling, motor vehicles and armored vehicles. In general, the benefits increase with the difficulty of applying external cooling to power electronics for reasons of space, weight, maintenance and cost.

Unfortunately, of all the SiC power electronics attributes, high temperature operation appears to be still elusive, because its implementation requires additional high temperature tolerance of device metallization, insulation and packaging and of passive components, which are also needed in a high temperature power circuit. Presently, a commonly accepted intermediate goal is to aim for 350 °C operation, which is still significantly lower than the SiC intrinsic device capability. In particular, a major obstacle is the achievement of long term reliability at this temperature of SiC DIMOS, IGBTs, MGTs and MCTs, because the gate oxide integrity decreases under high electric field stress and high temperature. Hence, high temperature applications of MOS-based SiC power devices are deferred to the future development of a more reliable MOS structure.

As it is normal for all new electronic technology applications, the development pace is determined by the achievement of lower cost, higher performance and improved reliability compared to existing alternatives. Therefore, we expect that SiC power electronic applications will expand with SiC device technology progress. Presently, not

all the SiC device types comply with the above requirements, and for this reason only simple devices, that is Schottky and PiN diodes, are being incorporated in applications. The most promising applications combine SiC diodes with Si switches, such as DMOS FETs and IGBTs, to provide higher efficiency at the system level for DC/DC power converters and motor drives. The major objective is to exploit the low switching losses associated with SiC diodes. Next, as fast SiC GTOs and JFETs will be developed, complete SiC half-bridge inverters will be built, which will provide the added advantage of higher temperature operation by avoiding the limitations of Si devices.

The SiC megawatt program at GE has made significant contributions to the development of SiC applications by investigating the applicability of SiC power devices to various GE power systems. In this context many promising power circuit applications have been proposed and analyzed. In addition, prototypes have been built if they could be implemented with SiC devices produced during this program. The most significant applications will be briefly described in the following sections.

5.2. High density power converters

DC/DC power converters are at the cornerstone of modern power electronic systems, because they allow to boost or reduce the main supply voltage to fit the needs of distributed subsystems. The main requirements are high efficiency and high density to minimize power loss and space allocated for the converters. Although these parameters depend on both the active and passive components, their values are mainly dependent on the frequency and temperature capabilities of the power devices, because in Si they are the most stringent among the circuit components [4].

As discussed in the previous section, SiC power devices lift these limitations allowing up to 10x higher frequency operation with low switching losses in the MHz range and in addition higher junction temperature in the 200-300 °C regime. Several key benefits result from this change. First, a high frequency design allows reducing the size of inductors and capacitors for a given power rating, thereby increasing the converter power density. Second, the combined effect of higher junction temperature and lower switching losses results in higher power efficiency, because less power is dissipated and it is disposed at higher rate due to the increased thermal difference between heat source and sink. Simulations have predicted a 50% power density improvement for a 100 V-2kV DC-DC boost converter by replacing Si with SiC [4]. The assumptions included a frequency change from 50 kHz to 500 kHz and a junction temperature change from 150 °C to 300 °C. The corresponding power density increased from 4 W/cm^3 to 7 W/cm^3 and the converter efficiency from 85% to 89% [4].

Figure 5-1 shows a low noise, high density 270 VDC to 10 VDC power converter built at GE CRD for avionic applications. The circuit topology, shown in Figure 5-2, is based on a full bridge design with one DIMOS FET for each branch and a primary transformer to modulate the input signal in a push-pull configuration. The output signal is derived from the bridge internal nodes and is rectified by two low voltage, fast recovery diodes. The problem is that with Si devices the secondary diode junction capacitance rings with the

transformer leakage inductance, causing EMI, overvoltages and stress on other components and limiting switching frequency. The transition to SiC enabled to solve this problem, because of the low reverse recovery time and small junction capacitance of the SiC diodes.

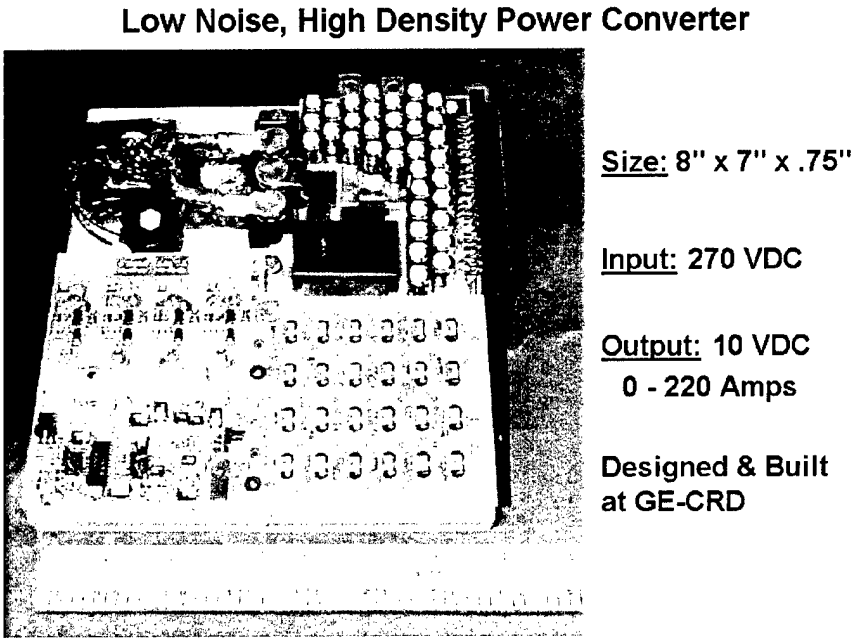


Figure 5-1. GE-CRD low noise, high density power converter.

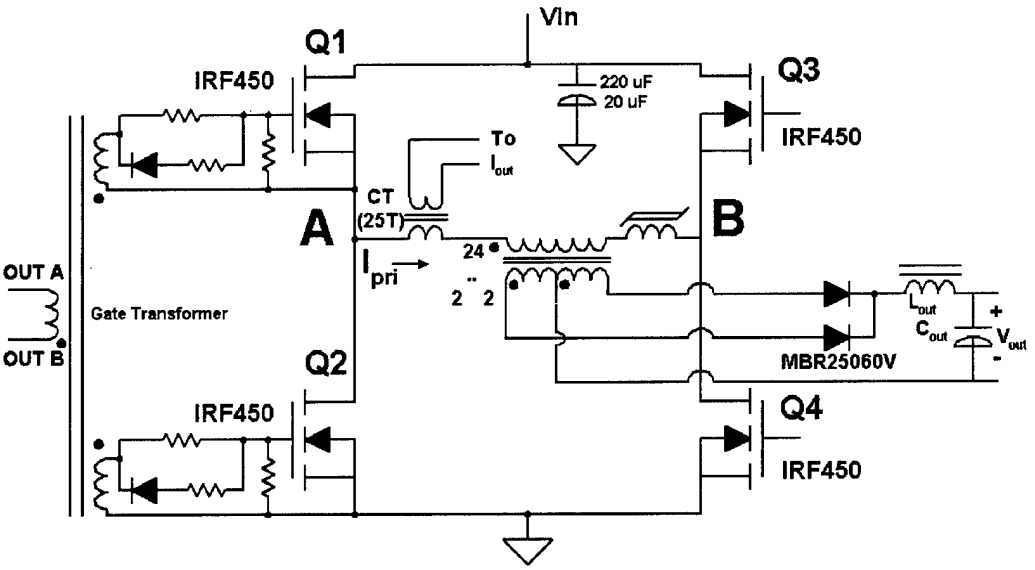


Figure 5-2. Circuit topology of high density converter.

5.3. Hybrid Si/SiC Inverter

Hybrid Si/SiC inverters are one of the earliest applications of SiC power diodes. They consist of replacing the flyback Si diodes with SiC Schottky or PiN diodes without changing the main switching devices, usually IGBTs [1-3,7,8]. A schematic diagram of a Si IGBT/SiC diode hybrid inverter is shown in Figure 5-3. The main advantage of using

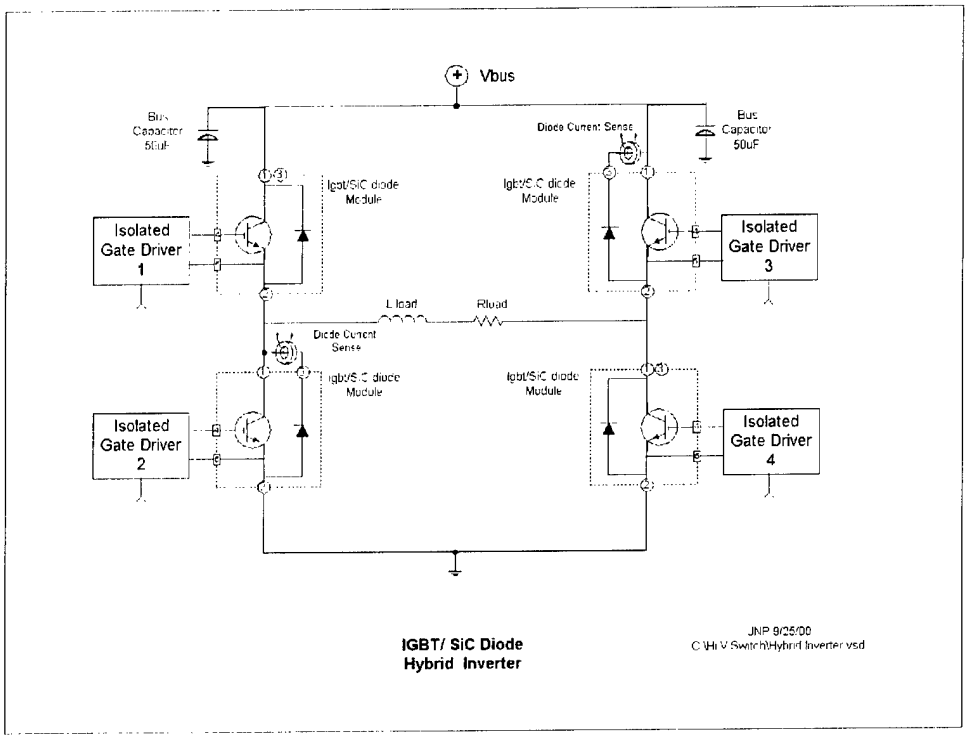


Figure 5-3. Si IGBT/SiC diode hybrid inverter.

a SiC diode for this circuit is its fast recovery characteristics that increases the freewheeling performance by operating at high frequency with low switching losses. Moreover, IGBT switching losses are also reduced, because a much smaller diode reverse recovery current is added to the IGBT current during turn-on with consequent lower stress on this device and higher di/dt rating.

The circuit schematic identifies four IGBT/diode modules, which represent the main circuit building blocks. To duplicate the hardware partitioning used for Si, GE and Powerex developed an integrated package for the basic inverter, which is shown in Figure 5-4. The purpose is to simplify circuit assembly by avoiding individual device handling. Each module consists of a 600 V, 75 A Si IGBT connected in parallel with a reverse polarity freewheeling 600 V, 20 A SiC rectifier. The latter consists of multiple SiC PiN diodes, fabricated at GE and connected in parallel by wire bonding to achieve a 20 A current rating.

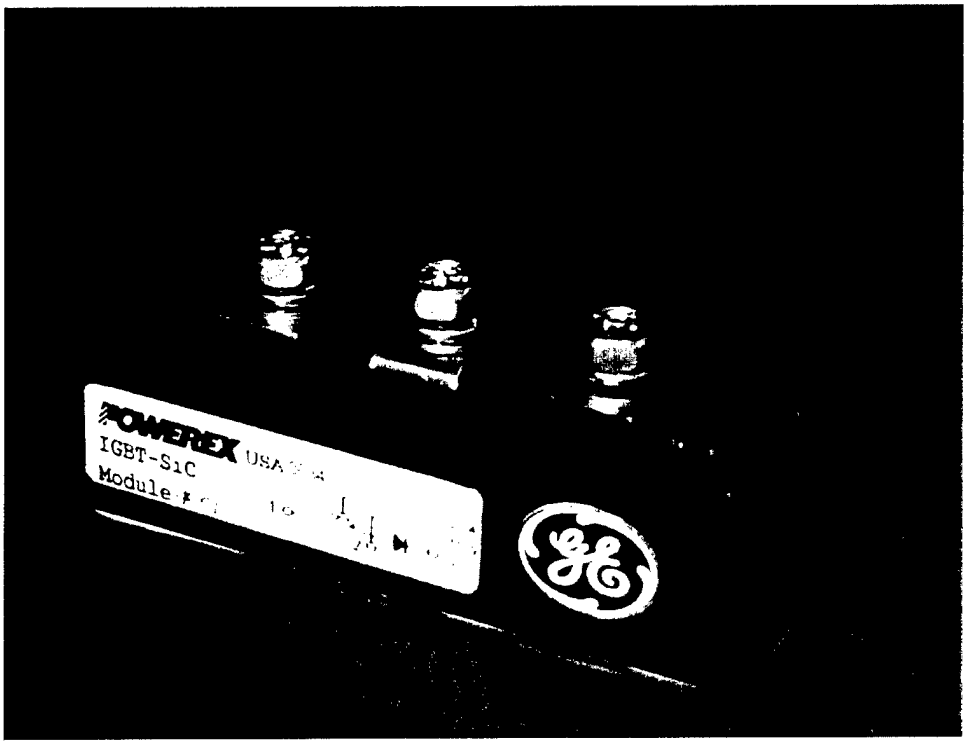


Figure 5-4. GE/Powerex integrated Si/SiC inverter module.

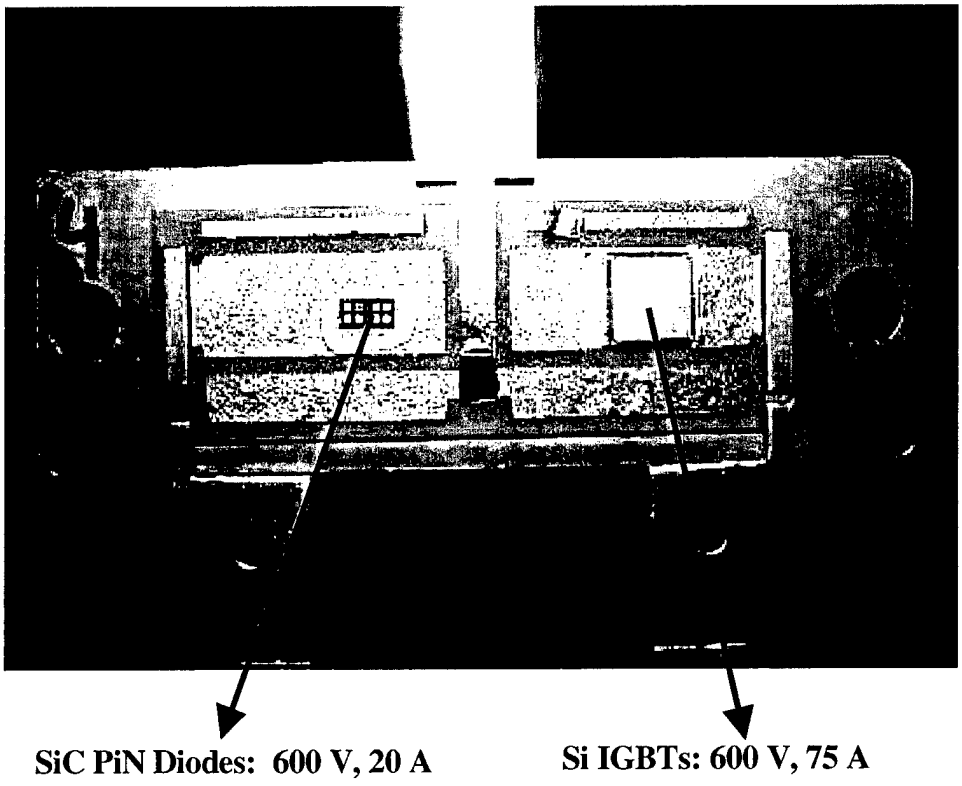


Figure 5-5. Interior of GE/Powerex Si/SiC power module.

The interior of the inverter power module is shown in Figure 5-5 after removal of the package cap. One can see on the left side a large die with multiple SiC diodes and on the right side the IGBT, which is distinguished by its larger footprint. There are three high current terminals. The central terminal connects together the SiC diode anode and the IGBT emitter, which are reachable from the top of the devices, while the side terminals contact separately the diode cathode and IGBT collector. This configuration allows monitoring the freewheeling diode current during testing or even during operation. Two additional low current terminals are available on the package for external connection to the gate driver, while internally they are connected to the IGBT gate and emitter.

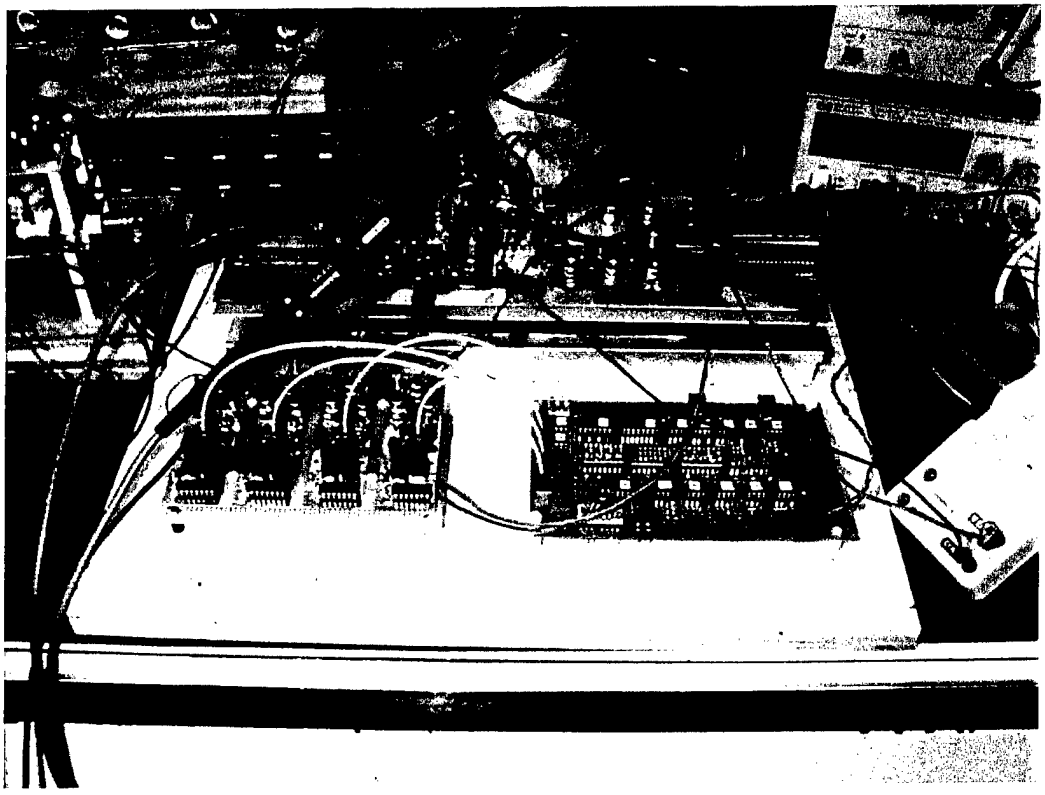


Figure 5-6. Breadboard hardware with control circuit and gate drivers.

A breadboard, shown in Figure 5-6, was built to characterize the hybrid Si/SiC inverter under various testing conditions. This breadboard contained control circuits and gate drivers to generate waveforms of various frequency, duty cycle, and amplitude to operate the hybrid Si/SiC inverter. The presence of stray inductance and capacitance associated with loose wiring connections strongly affected the efficiency measurements. As shown in Table 5-1, only for a bus voltage of 150 V and 200 V the hybrid Si/SiC inverter operated with higher efficiency than an equivalent all Si inverter. Consequently, these preliminary tests failed to demonstrate the advantages predicted by our simulations and by the literature. We conclude from these tests that to fully exploit the possibilities of the hybrid inverter it is necessary to design an appropriate circuit to operate at high frequency with low parasitics. Specifically, the frequency of 20 kHz used in these tests may have

been too low for taking full advantage of the low reverse recovery of the SiC diode. Additionally, replacing the SiC PiN diodes used here with SiC Schottky diodes with lower forward voltage drop may also improve the hybrid inverter efficiency.

Table 5-1. Hybrid Si/SiC efficiency test results.

DC Bus Voltage	100V	150V	200V	250V
Load Input Power	114W	250W	440W	690W
Hybrid Si/SiC Efficiency	**90.6%**	**96.3%**	**97.5%**	**97.8%**
All Si Inverter Efficiency	**92%**	**92.7%**	**95.5%**	**97.1%**

5.4. References

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6. Conclusion and Future Outlook

SiC power devices are an emerging technology with promising applications for high voltage, high power, high speed and high temperature operation. Great strides have been made in the past decade toward developing devices that meet, at least partially, these conditions. However, the low quality of SiC starting material, the high defect density, and the high cost of the wafers has limited the rate of progress. These factors have prevented until now the use of SiC power devices in various products, because of lower current rating and higher cost than Si devices. Fortunately, technological advances, such as those made during this program, have brought SiC power devices closer to their theoretical expectations and have increased the number of companies planning to launch SiC power products. Already Infineon and Cree have SiC power diodes available for prototype evaluation, while Sterling Semiconductor and Microsemi appear to be close followers.

The impact of this program on SiC power technology is documented in this report. The executive summary section contains an extensive discussion of the program objectives, technical approach, technical challenges, development tasks, program accomplishments, transition and scientific results. In conclusion, this program has advanced the SiC power device technology on many fronts spanning from devices to applications. Specifically, high performance PiN diodes, GTOs, DIMOS and MGTs were designed, simulated and characterized; manufacturable processes for PiN diodes and GTOs were developed; their static and dynamic performance was evaluated; Si and SiC hybrid half-bridge inverter modules were fabricated; and novel application concepts for SiC power devices were formulated and analyzed. The knowledge accumulated under this program was shared with the sponsor and the DoD community at first and then published to accelerate the technology transition.

The future of SiC power devices appears bright. The continued reduction of defect density, including micropipes, and the increase of wafer diameter are two important factors for increasing the chip size and consequently the current rating. The increase of epi thickness for both n- and p-type lightly doped layers will lead to higher voltage rating for PiN diodes and GTOs. As wafers with higher carrier lifetime will become available, it is expected that the lifetime will be tailored during the process to the device needs, as done for Si. Process technology will further evolve and adjust to the transition from the device demonstration phase to the manufacturing phase with increased attention being devoted to yield improvement and automated wafer handling to increase productivity and lower cost.

MOS SiC power devices are likely to trail the development of bipolar devices, because control of the MOS interface properties is still an obstacle toward their long term reliability. However, with progress in gate oxide formation and SiC surface preparation this problem will be solved in due time. There is nothing intrinsic to MOS SiC power device realization, which will be a fundamental block to their development. Nevertheless, because of the gate oxide properties, the operational envelope of MOS

power devices might be more limited than that of bipolar devices under equal reliability constraints.

Packaging is still an issue, especially for high temperature and high voltage operation. Since leakage current is thermally activated and increases with voltage stress, novel materials and packaging techniques must be developed to minimize parasitic effects and reliability loss. A parallel DARPA program at Rockwell Science Center has addressed packaging development for SiC megawatt power devices using innovative concepts based on refractory ceramic materials and phase transition heat exchange in special alloys. However, beyond discrete packaging, it is necessary to produce power device modules that are compatible with those used for silicon power devices. Our partner, Powerex, has produced a hybrid module, as mentioned before. Northrop Grumman has also developed a prototype power module. From these beginnings further work is required to develop a complete line of SiC power modules, which will fully exploit the capabilities of SiC power devices and will be responsive to the various application needs.

Looking further ahead, we anticipate the need to bridge the gap between SiC technology and computer-aided power circuit design. Presently, advanced circuit design methodology requires a full circuit behavior simulation before building a prototype. Consequently, accurate device models must be made available for the simulator of choice. Although SiC power device products are just beginning to reach the market, preliminary SiC device models should be developed soon for widely used simulators, such as SABRE, to provide a systematic evaluation of new application concepts using SiC and to compare them with alternative Si-based circuits. The results will lead to a rational choice of SiC or Si devices depending on applications and will optimize the system performance.